

Datasheet

Lyra 24P

Version 1.9

REVISION HISTORY

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CONTENTS

1	Introduction.....	5
1.1	Key Features.....	5
1.2	Hardware Features.....	6
1.3	Firmware Options.....	7
2	Ordering Information.....	7
3	System Overview.....	8
3.1	Block Diagram.....	8
3.2	EFR32BG24 SoC.....	9
3.3	Integrated Antenna.....	9
3.4	External Antenna.....	9
3.5	Power Supply.....	10
3.6	General Purpose Input / Output (GPIO).....	10
3.7	Security.....	10
4	Electrical Characteristics.....	13
4.1	Absolute Maximum Ratings.....	13
4.2	General Operating Conditions.....	14
4.3	MCU Current Consumption with 3 V Supply.....	15
4.4	Radio Current Consumption with 3 V Supply.....	16
4.5	RF Transmitter General Characteristics for the 2.4 GHz Band.....	17
4.6	RF Receiver General Characteristics for the 2.4 GHz Band.....	19
4.7	RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate.....	19
4.8	RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate.....	20
4.9	RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate.....	21
4.10	RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate.....	22
4.11	High-Frequency Crystal.....	24
4.12	Low-Frequency Crystal Oscillator.....	24
4.13	Precision Low Frequency RC Oscillator (LFRCO).....	25
4.14	GPIO Pins.....	26
4.15	Microcontroller Peripherals.....	27
4.16	Antenna Radiation and Efficiency for Lyra 24P Integrated Antenna.....	27
5	Reference Diagrams.....	30
5.1	Network Co-Processor (NCP) Application with UART Host.....	30
5.2	SoC Application.....	30
5.3	Boot.....	31
6	Pin Definitions.....	32
6.1	Lyra 24P 36-Pin PCB Module Pinout.....	32
6.2	Alternate Function Table.....	33
6.3	Analog Peripheral Connectivity.....	34
6.4	Digital Peripheral Connectivity.....	35
7	Design Guidelines.....	39
7.1	Layout and Placement.....	39
7.2	Proximity to Other Materials.....	41
7.3	Proximity to Human Body.....	41
7.4	Reset.....	41
7.5	Debug.....	41
7.6	Packet Trace Interface (PTI).....	41

7.7	Lyra 24P Module 50 Ohms RF Track Design for Connecting External Antenna with the Lyra 24P Module, 20dBm, RF Pad Variant (453-00148)	42
7.8	External Antenna Integration with the Lyra 24P Module, 20dBm, RF pad variant (453-00148).....	44
8	Mechanical Specifications	45
8.1	Dimensions (Lyra 24P series modules)	45
8.2	PCB Land Pattern (Lyra 24P series modules).....	46
8.3	Dimensions for 450-00184 Lyra 24P – Bluetooth v5.4 USB Adaptor (20dBm) with Integrated Antenna (Silicon Labs EFR32BG24).....	47
8.4	Lyra 24P Series Module Label Marking.....	48
8.5	Lyra 24P USB Adapter Label Marking.....	49
8.6	Lyra 24P USB Adapter Antenna Radiation Pattern	49
9	Soldering Recommendations.....	52
9.1	Reflow for lead Free Solder Paste.....	52
9.2	Recommended Reflow Profile for lead Free Solder Paste	52
10	Miscellaneous.....	53
10.1	Cleaning	53
10.2	Rework	53
10.3	Handling and Storage.....	53
11	Tape and Reel	54
12	Reliability Test	55
12.1	Climatic And Dynamic	55
12.2	Reliability MTBF Prediction	57
13	Regulatory	58
13.1	Regulatory information	58
13.2	Maximum Regulatory Certified RF TX Power per Country – 453-00148 Lyra 24P Series - Bluetooth v5.4 PCB Module (20dBm) with RF Trace Pad	59
13.3	Maximum Regulatory Certified RF TX Power per Country – 453-00145 Lyra 24P – Bluetooth v5.4 PCB Module (20dBm) with Integrated Antenna.....	69
13.4	Maximum Regulatory Certified RF TX Power per Country – 453-00184 Lyra 24P – Bluetooth v5.4 USB Adaptor (20dBm) with Integrated Antenna.....	78
13.5	Maximum Regulatory Certified RF TX Power per Country – 453-00142 Lyra 24P – Bluetooth v5.4 PCB Module (10dBm) with Integrated Antenna.....	79
14	Bluetooth SIG Qualification	85
14.1	Overview	85
14.2	Qualification Steps When Referencing on End Product Listing.....	85
15	Additional Information.....	87

1 INTRODUCTION

The Lyra 24P is a secure, high-performance wireless module optimized for the needs of battery and line powered IoT devices running on Bluetooth networks.

Based on the **Series 2 EFR32BG24 SoC**, it enables Bluetooth® Low Energy connectivity, delivering exceptional RF performance and energy efficiency, industry leading Secure Vault® technology, and future-proofing capabilities.

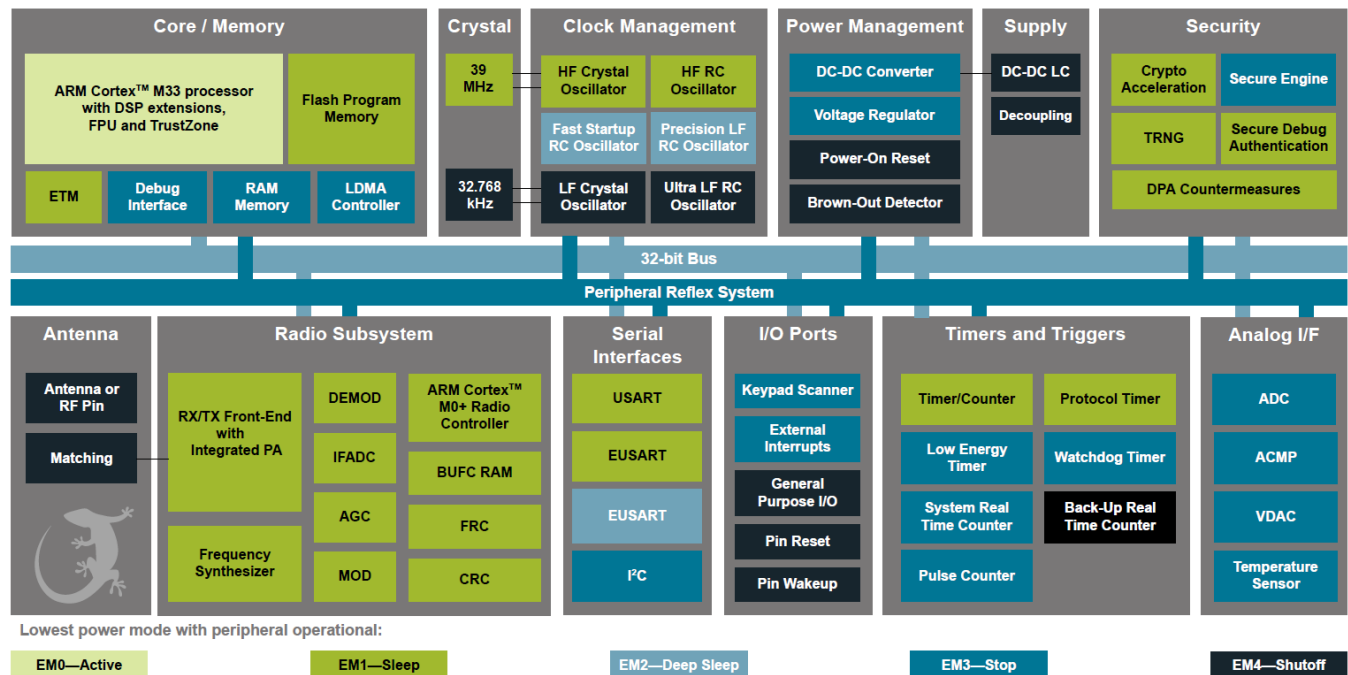
The Lyra 24P is a complete solution offered with robust and fully upgradeable software stacks, global regulatory certifications, advanced development and debugging tools, and documentation that simplifies and minimizes the development cycle of your end-product, helping to accelerate its time-to-market.

The Lyra 24P is intended for a broad range of applications, including:

- Smart Home Devices
- Lighting
- Building Automation and Security
- Gateways and Digital Assistants
- Bluetooth mesh Low Power Node

1.1 Key Features

- Bluetooth Low Energy 5.4
- Bluetooth Mesh connectivity
- Built-in antenna or RF pin
- +10 or +20 dBm TX output power (see 13.2, 13.3, and 13.5)
- -98.5 dBm BLE 1M RX sensitivity
- 32-bit ARM® Cortex®-M33 core at 39 MHz
- 1536/256 kB of Flash/RAM memory
- Vault High or Vault Mid security
- Rich set of analog and digital peripherals
- 26 GPIO pins
- -40 °C to 105 °C
- 12.9 mm x 15.0 mm



1.2 Hardware Features

- **Supported Protocols**
 - Bluetooth Low Energy (BLE) 5.4
 - Bluetooth Mesh
- **Wireless System-on-Chip**
 - 2.4 GHz radio
 - TX power up to +20 dBm (see 13.2, 13.3, and 13.5)
 - 32-bit ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
 - 1536 kB flash program memory 256 kB RAM data memory
 - Embedded Trace Macrocell (ETM) for advanced debugging
- **Receiver Sensitivity**
 - -106.5 dBm sensitivity (0.1% BER) at 125 kbps GFSK
 - -102.2 dBm sensitivity (0.1% BER) at 500 kbps GFSK
 - -98.5 dBm sensitivity (0.1% BER) at 1 Mbps GFSK
 - -95.7 dBm sensitivity (0.1% BER) at 2 Mbps GFSK
- **Current Consumption**
 - 4.5 mA RX current at 1 Mbps GFSK
 - 4.8 mA TX current at 0 dBm (BGM240Px22)
 - 18.8 mA TX current at 10 dBm (BGM240Px22)
 - 154.8 mA TX current at 19.6 dBm (BGM240Px32)
 - 33.4 μ A/MHz in Active Mode (EM0) at 39.0 MHz
 - 1.3 μ A EM2 DeepSleep current (16 kB RAM retention and RTC running from LFRCO)
- **Regulatory Certifications**
 - CE (EU)
 - UKCA (UK)
 - FCC (USA)
 - ISED (Canada)
 - MIC (Japan)
 - KC (South Korea)
 - AS/NZ (Australia, New Zealand)
- **Operating Range**
 - 1.8 to 3.8 V
 - -40 to +105°C
- **Dimensions**
 - 12.9 mm x 15.0 mm x 2.15 mm
- **Security**
 - Secure Boot with Root of Trust and Secure Loader (RTSL)
 - Hardware Cryptographic Acceleration with DPA countermeasures for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, and ECDH
 - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
 - ARM® TrustZone®
 - Secure Debug Interface lock/unlock Secure Key Management with PUF Anti-Tamper
 - Secure Attestation
- **MCU Peripherals**
 - Analog to Digital Converter (ADC)
 - 12-bit @ 1 Msps
 - 16-bit @ 76.9 kpsps
 - 2 x Analog Comparator (ACMP)
 - 2 x Digital to Analog Converter (VDAC)
 - Up to 26 General Purpose I/O pins with output state retention and asynchronous interrupts
 - 8 Channel DMA Controller
 - 16 Channel Peripheral Reflex System (PRS)
 - 3 x 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
 - 2 x 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
 - 2 x 32-bit Real Time Counter (SYSRTC/BURTC)
 - 24-bit Low Energy Timer for waveform generation (LETIMER)
 - 16-bit Pulse Counter with asynchronous operation (PCNT) 2 x Watchdog Timer (WDOG)
 - 1 x Universal Synchronous/Asynchronous Receiver/Transmitter (USART), supporting UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
 - 2 x Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART) supporting UART/SPI/DALI/ IrDA
 - 2 x I2C interface with SMBus support
 - Low-Frequency RC Oscillator with precision mode to replace 32 kHz sleep crystal (LFRCO)
 - Keypad scanner supporting up to 6x8 matrix (KEYSCAN)
 - Die temperature sensor with $\pm 1.5^\circ\text{C}$ accuracy after single point calibration

1.3 Firmware Options

The Lyra 24P series supports two different firmware options for software development:

AT Command Set – fully featured and extensible to suit any developer’s needs.

- Proven over 5+ years
- Basic Bluetooth LE cable replacement
- Simplest implementation possible

C Code – Full software development with Silicon Labs SDK and Toolchain

- Native C code development
- Use Simplicity Studio IDE
- Full functionality of Silicon Labs HW / SW

2 ORDERING INFORMATION

Table 1: Ordering Information

Part	Description
453-00142R	Lyra 24P Series - Bluetooth v5.4 PCB Module (10dBm) with integrated antenna (Silicon Labs EFR32BG24) - Tape / Reel
453-00142C	Lyra 24P Series - Bluetooth v5.4 PCB Module (10dBm) with integrated antenna (Silicon Labs EFR32BG24) – Cut / Tape
453-00145R	Lyra 24P Series - Bluetooth v5.4 PCB Module (20dBm) with integrated antenna (Silicon Labs EFR32BG24) - Tape / Reel
453-00145C	Lyra 24P Series - Bluetooth v5.4 PCB Module (20dBm) with integrated antenna (Silicon Labs EFR32BG24) – Cut / Tape
453-00148R	Lyra 24P Series - Bluetooth v5.4 PCB Module (20dBm) with RF Trace Pad (Silicon Labs EFR32BG24) - Tape / Reel
453-00148C	Lyra 24P Series - Bluetooth v5.4 PCB Module (20dBm) with RF Trace Pad (Silicon Labs EFR32BG24) – Cut / Tape
453-00142-K1	Lyra 24P Series - Development Kit - Bluetooth v5.4 PCB Module (10dBm) with integrated antenna
453-00145-K1	Lyra 24P Series - Development Kit - Bluetooth v5.4 PCB Module (20dBm) with integrated antenna
453-00148-K1	Lyra 24P Series - Development Kit - Bluetooth v5.4 PCB Module (20dBm) with RF Trace Pad
450-00184	Lyra 24P Series - Bluetooth v5.4 USB Adapter (20dBm) with integrated antenna (Silicon Labs EFR32BG24)

Note:

1. Lyra 24P series modules operate in the 2.4 GHz ISM frequency band.
2. The maximum RF TX power allowed by different regional regulatory authorities may differ from the maximum output power a module can produce. End-product manufacturers must then verify that the module is configured to meet the regulatory limits for each region in accordance with the local rules and the formal certification test reports.
3. See section 13.2, 13.3, and 13.5 per Lyra 24P module part number.
4. Lyra 24P modules are pre-programmed with **Lyra 24P BGAPI UART/OTA DFU** bootloader. Lyra 24P AT firmware can be loaded by the customer (via SWD interface or via boot loader (UART or OTA)). Lyra 24P USB dongle ships with bootloader and AT firmware.

3 SYSTEM OVERVIEW

3.1 Block Diagram

The Lyra 24P module is a highly-integrated, high-performance system with all the hardware components needed to enable 2.4 GHz wireless connectivity and support robust networking capabilities via multiple wireless protocols.

Built around the **EFR32BG24** Wireless SoC, the Lyra 24P includes a built-in antenna, an RF matching network (optimized for transmit power efficiency), supply decoupling and filtering components, an LC tank for DC-DC conversion, a 39 MHz reference crystal, and an RF shield. Also, it supports the use of an external 32 kHz crystal as a low frequency reference signal via GPIO pins for use cases demanding maximum energy efficiency.

For designs where an external antenna solution may be beneficial, a module variant with a 50 Ω-matched RF pin instead of the built-in antenna is available (**for Lyra 24P, RF, 20dBm, RF Trace only**).

Because the RF matching network is optimized for transmit power efficiency, modules rated for +20 dBm will show non-optimal current consumption and performance when operated at a lower output power (i.e. +10 or 0 dBm).

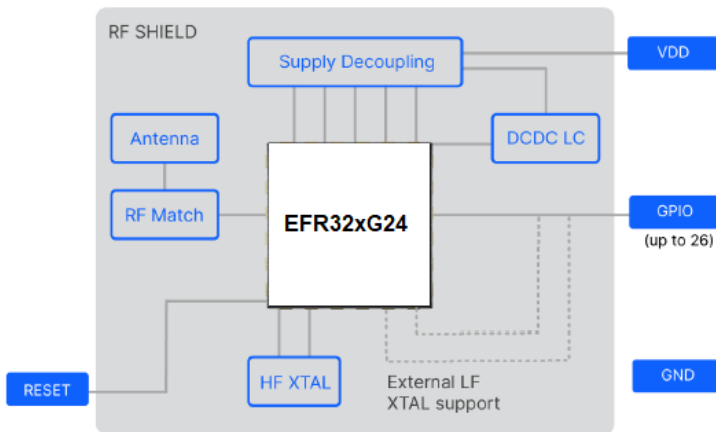


Figure 3: Lyra 24P Block Diagram – Built-in Antenna Variant

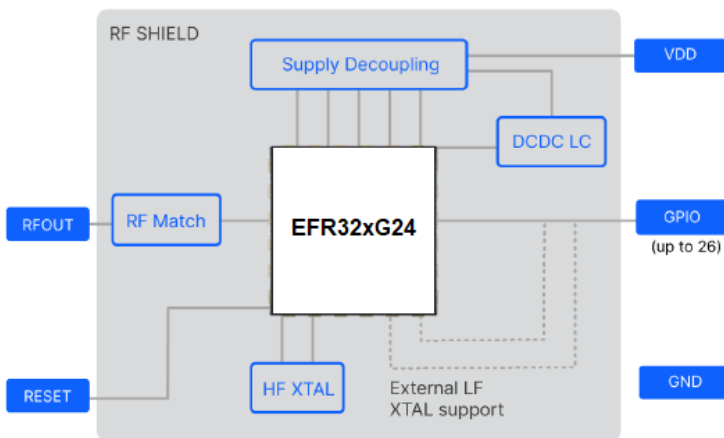


Figure 4: Lyra 24P Block Diagram – RF Pin Variant

A simplified internal schematic for the Lyra 24P module is shown in Figure 5.

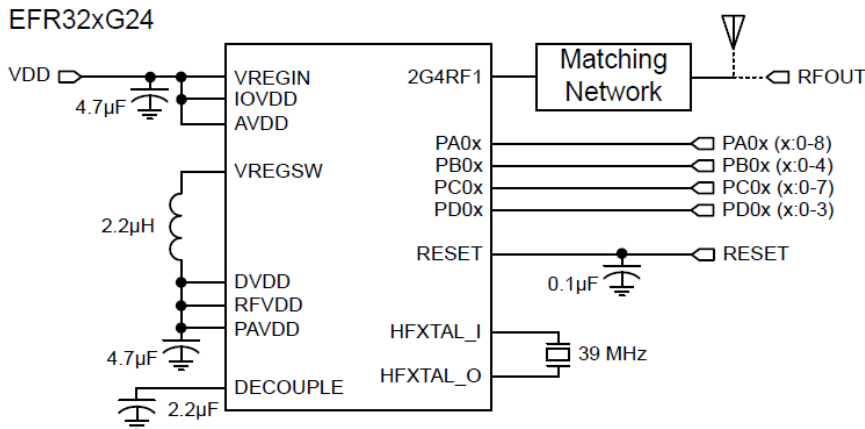


Figure 5: Lyra 24P Module Schematic

3.2 EFR32BG24 SoC

The **EFR32BG24** SoC features a 32-bit ARM Cortex M33 core, a 2.4 GHz high-performance radio, 1536 kB of Flash memory, 256 kB of RAM, a dedicated core for security, a rich set of MCU peripherals, and various clock management and serial interfacing options. See the [EFR32xG24 Reference Manual](#) and [EFR32BG24 Data Sheet](#) for details.

3.3 Integrated Antenna

Lyra 24P modules come with two antenna solutions variants: A built-in antenna or a 50 Ohms matched RF pin to support an external antenna. Typical performance characteristics of the built-in antenna are detailed in table below.

Table 2: Integrated Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	-1 dB	Antenna efficiency, gain, and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to Design Guidelines for recommendations to achieve optimal antenna performance.
Peak gain	1.82 dBi	

3.4 External Antenna

Lyra 24P module can be used with external antennas (certified by Laird Connectivity) and requires a RF 50 Ohm track (Ground Coplanar Waveguide) to be designed to run from Lyra 24P module RFOUT (pin 33) to an RF antenna connector (IPEX MHF 4) on the host PCB. The 50 ohm RF track design and length **MUST** be copied as defined in section [Lyra 24P Module 50 Ohms RF Track Design for Connecting External Antenna with the Lyra 24P Module, 20dBm, RF Pad Variant \(453-00148\)](#).

The list of supported external antennas (certified by Laird Connectivity) are listed in section [External Antenna Integration with the Lyra 24P Module](#).

3.5 Power Supply

The Lyra 24P requires a single nominal supply level (VDD) to operate and supports an operating range of 1.8 to 3.8 V. The nominal level needed for **+10 dBm devices** (part number: 453-00142) is **3.0 V** whereas **+20 dBm devices** (part number: 453-00145 and 453-00148) **require 3.3 V** in order to achieve higher TX output power. All necessary decoupling, filtering and DC-DC-related components are included in the module.

Note: The power amplifier for +10 dBm modules is supplied through an internal LDO, and thus is independent of the VDD supply. Respectively, the power amplifier for +20 dBm modules is supplied through the VDD pin with a target level of 3.3 V.

3.6 General Purpose Input / Output (GPIO)

The Lyra 24P has up to 26 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have EM4 wake functionality. These pins are listed in [Table 19: GPIO Alternate Function Table](#).

3.7 Security

Lyra 24P modules support one of two levels in the Security Portfolio offered by Silicon Labs: **Secure Vault Mid** or **Secure Vault High**. Lyra 24P modules support Secure Vault High.

Secure Vault is a collection of technologies that deliver state-of-the-art security and upgradability features to protect and futureproof IoT devices against costly threats, attacks, and tampering. A dedicated security CPU enables the Secure Vault functions and isolates cryptographic functions and data from the Cortex-M33 core. Lyra 24P part numbers support Secure Vault High.

Table 3: Secure Vault Features

Feature	Secure Vault Mid	Secure Vault High
True Random Number Generator (TRNG)	Yes	Yes
Secure Boot with Root of Trust and Secure Loader (RTSL)	Yes	Yes
Secure Debug with Lock/Unlock	Yes	Yes
DPA Countermeasures	Yes	Yes
Anti-Tamper		Yes
Secure Attestation		Yes
Secure Key Management		Yes
Symmetric Encryption	<ul style="list-style-type: none"> AES 128 / 192 / 256 bit ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC 	<ul style="list-style-type: none"> AES 128 / 192 / 256 bit ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC ChaCha20
Public Key Encryption - ECDSA / ECDH / EdDSA	<ul style="list-style-type: none"> p192 and p256 	<ul style="list-style-type: none"> p192, p256, p384 and p521 Curve25519 (ECDH) Ed25519 (EdDSA)

Feature	Secure Vault Mid	Secure Vault High
Key Derivation	<ul style="list-style-type: none"> • ECJ-PAKE p192 and p256 	<ul style="list-style-type: none"> • ECJ-PAKE p192, p256, p384, and p521 • PBKDF2 • HKDF
Hashes	<ul style="list-style-type: none"> • SHA-1 • SHA-2/256 	<ul style="list-style-type: none"> • SHA-1 • SHA-2 256, 384, and 512 • Poly1305

3.7.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates. For more information about this feature, see [AN1218: Series 2 Secure Boot with RTSL](#).

3.7.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations, and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CCM (Counter with CBC-MAC)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192, P-256, P-384, and P-521 for ECDH (Elliptic Curve Diffie-Hellman) key derivation, and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for EdDSA (Edwards-curve Digital Signature Algorithm) sign and verify operations.

Secure Vault also supports ECJ-PAKE (Elliptic Curve variant of Password Authenticated Key Exchange by Juggling) and PBKDF2 (Password-Based Key Derivation Function 2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

3.7.3 True Random Number Generator

The True Random Number Generator module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31 as well as online health tests required for NIST SP800-90C.

The **TRNG** is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.7.4 Secure Debug with Lock / Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

In addition, Secure Vault High also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end- user data.

For more information about this feature, see [AN1190: Series 2 Secure Debug](#).

3.7.5 DPA Countermeasures

The AES and ECC accelerators have Differential Power Analysis (DPA) countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

3.7.6 Secure Key Management with PUF

Key material in Secure Vault High products is protected by "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of protecting a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33, which includes off-chip storage as well. The symmetric key used for this wrapping and unwrapping must be highly secure because it can expose all other key materials in the system. The Secure Vault Key Management system uses a Physically Unclonable Function (PUF) to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

3.7.7 Anti-Tamper

Secure Vault High devices provide internal tamper protection which monitors parameters such as voltage, temperature, and electromagnetic pulses as well as detecting tamper of the security sub-system itself. Additionally, eight external configurable tamper pins support external tamper sources, such as enclosure tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all protected key materials un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

For more information about this feature, see [AN1247: Anti-Tamper Protection Configuration and Use](#).

3.7.8 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate, which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

The secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

For more information about this feature, see [AN1268: Authenticating Silicon Labs Devices Using Device Certificates](#).

4 ELECTRICAL CHARACTERISTICS

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_A=25\text{ °C}$ and **VDD supply at 3.0 V**, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

4.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	+105	°C
Voltage on VDD supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on VDD supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V/ μ s
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	$V_{VDD}+0.3$	V
DC voltage on RESETn pin ¹	V_{RESETn}		-0.3	—	3.8	V
Absolute voltage on RFOUT pin	V_{MAX2G4}		-0.3	—	$V_{VDD}+0.3$	V
Total current into VDD pin	I_{VDDMAX}	Source	—	—	200	mA
Total current into GND pin	I_{GNDMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

1. The RESETn pin has a pull-up device to the internal DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VDD when DC-DC is inactive.

4.2 General Operating Conditions

Table 5: General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A		-40	—	+105	°C
VDD operating supply voltage	V_{VDD}	10 dBm Module, DC-DC in regulation	2.2	3.0	3.8	V
		20 dBm Module, DC-DC in regulation	2.2	3.3	3.8	V
		10 dBm Module, DC-DC in bypass	1.8	3.0	3.8	V
		20 dBm Module, DC-DC in bypass	1.8	3.3	3.8	V
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	78	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
PCLK frequency	f_{PCLK}	VSCALE2 or VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	78	MHz
		VSCALE1	—	—	40	MHz
EM01 Group C clock frequency	$f_{EM01GRPBCLK}$	VSCALE2	—	—	78	MHz
		VSCALE1	—	—	40	MHz
Radio HCLK frequency	f_{RHCLK}	VSCALE2 or VSCALE1	—	39.0	—	MHz

4.3 MCU Current Consumption with 3 V Supply

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation. Voltage scaling level = VSCALE1. T_A = 25 °C.** Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 6: MCU Current Consumption with 3 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2	—	33.3	—	μA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2	—	32.8	—	μA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	49.1	—	μA/MHz
		39 MHz crystal, CPU running Prime from flash	—	33.9	—	μA/MHz
		39 MHz crystal, CPU running while loop from flash	—	33.4	—	μA/MHz
		39 MHz crystal, CPU running CoreMark loop from flash	—	49.4	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	28.1	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2	—	22.6	—	μA/MHz
		39 MHz crystal	—	24.4	—	μA/MHz
		38 MHz HFRCO	—	19.0	—	μA/MHz
Current consumption in EM2 mode, VSCALE0	I _{EM2_VS}	256 kB RAM and full Radio RAM retention, RTC running from LFXO ¹	—	2.9	—	μA
		256 kB RAM and full Radio RAM retention, RTC running from LFRCO ¹	—	2.9	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFXO ¹	—	1.3	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO ¹	—	1.3	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO in precision mode ¹	—	1.9	—	μA
	I _{EM3_VS}	256 kB RAM and full Radio RAM retention, RTC running from ULFRCO ¹	—	2.7	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM3 mode, VSCALE0		16 kB RAM and full Radio RAM retention, RTC running from ULFRCO ¹	—	1.1	—	μA
Current consumption in EM4 mode	I _{EM4}	No BURTC, No LF Oscillator	—	0.27	—	μA
		BURTC with LXO	—	0.64	—	μA
Current consumption during reset	I _{RST}	Hard pin reset held	—	467	—	μA

Note:

1. CPU cache retained, EM0/EM1 peripheral states retained.

4.4 Radio Current Consumption with 3 V Supply

RF current consumption measured with MCU in EM1 and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation. T_A = 25 °C.**

Table 7: Radio Current Consumption with 3.0 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception, VSCALE1, EM1P	I _{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	4.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	4.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	4.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	5.2	—	mA
Current consumption in receive mode, listening for packet, VSCALE1, EM1P	I _{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	4.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	4.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	4.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	5.2	—	mA
Current consumption in transmit mode	I _{TX}	f = 2.4 GHz, CW, 0 dBm output power	—	4.8	—	mA
		f = 2.4 GHz, CW, +10 dBm output power	—	18.8	—	mA
		f = 2.4 GHz, CW, +20 dBm output power, VDD = 3.3 V ¹	—	154.8	—	mA

Note:

1. Maximum output power for Bluetooth Low Energy is limited to 19.6 dBm for compliance with the Bluetooth Core Specifications.

4.5 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation**. RF center frequency **2.45 GHz**. **T_A=25°C**.

Table 8: RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition (Output Power)	Min	Typ	Max	Unit
RF tuning frequency range	F _{RANGE}		2402	—	2480	MHz
Maximum TX power	POUT _{MAX}	0 dBm	—	-0.3	—	dBm
		+10 dBm	—	10	—	dBm
		+20 dBm, VDD = 3.3 V ¹	—	19.6	—	dBm
Minimum active TX Power	POUT _{MIN}	0 dBm	—	-24	—	dBm
		+10 dBm	—	-30	—	dBm
		+20 dBm, VDD = 3.3 V	—	-33.7	—	dBm
Output power step size	POUT _{STEP}	0 dBm	0.1	0.7	9.9	dBm
		+10 dBm, -5 dBm < Output power < 0 dBm	0.6	1.1	1.8	dBm
		+10 dBm, 0 dBm < Output power < 10 dBm	0.1	0.3	0.8	dBm
		+20 dBm, VDD = 3.3 V, Output power < 0 dBm	0.9	3.6	14.4	dBm
		+20 dBm, 0 dBm < Output power < 20 dBm	0.1	0.2	1.3	dBm
Output power variation vs VDD supply voltage variation, frequency = 2450 MHz	POUT _{VAR_V}	0 dBm with VDD voltage swept from 1.8 V to 3.8 V	—	0.01	—	dB
		+10 dBm with VDD voltage swept from 1.8 V to 3.8 V	—	0.05	—	dB
		+20 dBm with VDD voltage swept from 1.8 V to 3.8 V	—	5.4	—	dB
Output power variation vs temperature, Frequency = 2450 MHz	POUT _{VAR_T}	0 dBm, (-40 to +105 °C)	—	1.0	—	dB
		+10 dBm, (-40 to +105 °C)	—	0.3	—	dB
		+20 dBm, VDD = 3.3 V, (-40 to +105 °C)	—	0.2	—	dB
Output power variation vs RF frequency	POUT _{VAR_F}	0 dBm	—	0.2	—	dB
		+10 dBm	—	0.2	—	dB
		+20 dBm, VDD = 3.3 V	—	0.2	—	dB

Note:

1. Maximum output power for Bluetooth Low Energy is limited to 19.6 dBm for compliance with the Bluetooth Core Specifications.

4.6 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation.** RF center frequency **2.45 GHz.** **T_A = 25°C.**

Table 9: RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F _{RANGE}		2402	—	2480	MHz

4.7 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation.** RF center frequency **2.45 GHz.** **T_A = 25°C.**

Table 10: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal ¹	—	10	—	dBm
Sensitivity	SENS	+10 dBm Module, Signal is reference signal, 37 byte payload ¹	—	-98.5	—	dBm
		+10 dBm Module, Signal is reference signal, 255 byte payload ¹	—	-96.9	—	dBm
		+10 dBm Module, With non-ideal signals ^{2 1}	—	-96.5	—	dBm
		+20 dBm Module, Signal is reference signal, 37 byte payload ¹	—	-97.6	—	dBm
		+20 dBm Module, Signal is reference signal, 255 byte payload ¹	—	-96	—	dBm
		+20 dBm Module, With non-ideal signals ^{2 1}	—	-95.6	—	dBm
Signal to co-channel interferer	C/I _{CC}	(see notes) ^{1 3}	—	8.7	—	dB
N ± 1 Adjacent channel selectivity	C/I ₁	Interferer is reference signal at +1 MHz offset ^{1 3 4 5}	—	-5.4	—	dB
		Interferer is reference signal at -1 MHz offset ^{1 3 4 5}	—	-5.3	—	dB
N ± 2 Alternate channel selectivity	C/I ₂	Interferer is reference signal at +2 MHz offset ^{1 3 4 5}	—	-40.9	—	dB
		Interferer is reference signal at -2 MHz offset ^{1 3 4 5}	—	-39.7	—	dB
N ± 3 Alternate channel selectivity	C/I ₃	Interferer is reference signal at +3 MHz offset ^{1 3 4 5}	—	-45.5	—	dB
		Interferer is reference signal at -3 MHz	—	-45.7	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
		offset ^{1 3 4 5}				
Selectivity to image frequency	C/I _{IM}	Interferer is reference signal at image frequency with 1 MHz precision ^{1 5}	—	-23.3	—	dB
Selectivity to image frequency ± 1 MHz	C/I _{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision ^{1 5}	—	-40.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision ^{1 5}	—	-5.4	—	dB
Intermodulation performance	IM	n = 3 (see note ⁶)	—	-17.3	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -67 dBm.
4. Desired frequency 2402 MHz ≤ F_c ≤ 2480 MHz.
5. With allowed exceptions.
6. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.8 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation.** RF center frequency **2.45 GHz.** T_A = 25 °C.

Table 11: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal ¹	—	10	—	dBm
Sensitivity	SENS	+10 dBm Module, Signal is reference signal, 37 byte payload ¹	—	-95.7	—	dBm
		+10 dBm Module, Signal is reference signal, 255 byte payload ¹	—	-94.2	—	dBm
		+10 dBm Module, With non-ideal signals ^{2 1}	—	-93.9	—	dBm
		+20 dBm Module, Signal is reference signal, 37 byte payload ¹	—	-94.8	—	dBm
		+20 dBm Module, Signal is reference signal, 255 byte payload ¹	—	-93.3	—	dBm
		+20 dBm Module, With non-ideal signals ^{2 1}	—	-93.1	—	dBm
Signal to co-channel interferer	C/I _{CC}	(see notes) ^{1 3}	—	8.6	—	dB
N ± 1 Adjacent channel selectivity	C/I ₁	Interferer is reference signal at +2 MHz offset ^{1 5 4 3}	—	-5.3	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
		Interferer is reference signal at -2 MHz offset ^{1 5 4 3}	—	-5.8	—	dB
N ± 2 Alternate channel selectivity	C/I ₂	Interferer is reference signal at +4 MHz offset ^{1 5 4 3}	—	-42.2	—	dB
		Interferer is reference signal at -4 MHz offset ^{1 5 4 3}	—	-44.2	—	dB
N ± 3 Alternate channel selectivity	C/I ₃	Interferer is reference signal at +6 MHz offset ^{1 5 4 3}	—	-48.1	—	dB
		Interferer is reference signal at -6 MHz offset ^{1 5 4 3}	—	-50.2	—	dB
Selectivity to image frequency	C/I _{IM}	Interferer is reference signal at image frequency with 1 MHz precision ^{1 5}	—	-22.8	—	dB
Selectivity to image frequency ± 2 MHz	C/I _{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision ^{1 5}	—	-42.2	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision ^{1 5}	—	-5.3	—	dB
Intermodulation performance	IM	n = 3 (see note ⁶)	—	-18.3	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -64 dBm.
4. Desired frequency 2402 MHz ≤ F_c ≤ 2480 MHz.
5. With allowed exceptions.
6. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.9 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation.** RF center frequency **2.45 GHz.** T_A = 25 °C.

Table 12: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal ¹	—	10	—	dBm
Sensitivity	SENS	+10 dBm Module, Signal is reference signal, 37 byte payload ¹	—	-102.2	—	dBm
		+10 dBm Module, Signal is reference signal, 255 byte payload ¹	—	-101	—	dBm
		+10 dBm Module, With non-ideal signals ^{2 1}	—	-100	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
		+20 dBm Module, Signal is reference signal, 37 byte payload ¹	—	-101.4	—	dBm
		+20 dBm Module, Signal is reference signal, 255 byte payload ¹	—	-100	—	dBm
		+20 dBm Module, With non-ideal signals ^{2 1}	—	-99	—	dBm
Signal to co-channel interferer	C/I _{CC}	(see notes) ^{1 3}	—	2.7	—	dB
N ± 1 Adjacent channel selectivity	C/I ₁	Interferer is reference signal at +1 MHz offset ^{1 3} 4 5	—	-7.1	—	dB
		Interferer is reference signal at -1 MHz offset ^{1 3} 4 5	—	-7.4	—	dB
N ± 2 Alternate channel selectivity	C/I ₂	Interferer is reference signal at +2 MHz offset ^{1 3} 4 5	—	-46.8	—	dB
		Interferer is reference signal at -2 MHz offset ^{1 3} 4 5	—	-49.7	—	dB
N ± 3 Alternate channel selectivity	C/I ₃	Interferer is reference signal at +3 MHz offset ^{1 3} 4 5	—	-49.4	—	dB
		Interferer is reference signal at -3 MHz offset ^{1 3} 4 5	—	-54.5	—	dB
Selectivity to image frequency	C/I _{IM}	Interferer is reference signal at image frequency with 1 MHz precision ^{1 5}	—	-49	—	dB
Selectivity to image frequency ± 1 MHz	C/I _{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision ^{1 5}	—	-49.4	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision ^{1 5}	—	-46.8	—	dB

Note:

1. 0.017% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -72 dBm.
4. Desired frequency 2402 MHz ≤ F_c ≤ 2480 MHz.
5. With allowed exceptions.

4.10 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation.** RF center frequency **2.45 GHz.** T_A = 25 °C.

Table 13: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable	SAT	Signal is reference signal ¹	—	10	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
receiver input level						
Sensitivity	SENS	+10 dBm Module, Signal is reference signal, 37 byte payload ¹	—	-106.5	—	dBm
		+10 dBm Module, Signal is reference signal, 255 byte payload ¹	—	-106.1	—	dBm
		+10 dBm Module, With non-ideal signals ^{2 1}	—	-105.7	—	dBm
		+20 dBm Module, Signal is reference signal, 37 byte payload ¹	—	-105.6	—	dBm
		+20 dBm Module, Signal is reference signal, 255 byte payload ¹	—	-105.3	—	dBm
		+20 dBm Module, With non-ideal signals ^{2 1}	—	-104.8	—	dBm
Signal to co-channel interferer	C/I _{CC}	(see notes) ^{1 3}	—	0.9	—	dB
N ± 1 Adjacent channel selectivity	C/I ₁	Interferer is reference signal at +1 MHz offset ^{1 3 4 5}	—	-12.4	—	dB
		Interferer is reference signal at -1 MHz offset ^{1 3 4 5}	—	-12.8	—	dB
N ± 2 Alternate channel selectivity	C/I ₂	Interferer is reference signal at +2 MHz offset ^{1 3 4 5}	—	-52.6	—	dB
		Interferer is reference signal at -2 MHz offset ^{1 3 4 5}	—	-55.5	—	dB
N ± 3 Alternate channel selectivity	C/I ₃	Interferer is reference signal at +3 MHz offset ^{1 3 4 5}	—	-53.8	—	dB
		Interferer is reference signal at -3 MHz offset ^{1 3 4 5}	—	-60.0	—	dB
Selectivity to image frequency	C/I _{IM}	Interferer is reference signal at image frequency with 1 MHz precision ^{1 5}	—	-53.0	—	dB
Selectivity to image frequency ± 1 MHz	C/I _{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision ^{1 5}	—	-53.8	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision ^{1 5}	—	-52.6	—	dB

Note:

1. 0.017% Bit Error Rate.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1						
3. Desired signal -79 dBm.						
4. Desired frequency $2402 \text{ MHz} \leq F_c \leq 2480 \text{ MHz}$.						
5. With allowed exceptions.						

4.11 High-Frequency Crystal

Table 14: High-Frequency Crystal

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXTAL}		—	39	—	MHz
Initial calibrated accuracy	$\text{ACC}_{\text{HFXTAL}}$		-10	±5	10	ppm
Temperature drift	$\text{DRIFT}_{\text{HFXTAL}}$	Across specified temperature range	-20	—	20	ppm

4.12 Low-Frequency Crystal Oscillator

Table 15: Low-Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	kOhms
		GAIN = 1 to 3	—	—	100	kOhms
Supported range of crystal load capacitance ¹	CL_{LFXO}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note2)	10	—	12.5	pF
		GAIN = 3 (see note2)	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kΩ, CL = 12.5pF, GAIN ³ = 2, AGC ⁴ = 1	—	294	—	nA
Startup Time	T_{STARTUP}	ESR = 70 kΩ, CL = 7pF, GAIN ³ = 1, AGC ⁴ = 1	—	52	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting ⁵	$\text{CL}_{\text{LFXO_MIN}}$	CAPTUNE=0	—	5.2	—	pF
On-chip tuning capacitor value at maximum setting ⁵	$\text{CL}_{\text{LFXO_MAX}}$	CAPTUNE=0x4F	—	26.2	—	pF

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap, and the two caps will be seen in series by the crystal						

4.13 Precision Low Frequency RC Oscillator (LFRCO)

Table 16: Precision Low Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}	Normal mode	-3	—	3	%
		Precision mode ¹ , across operating temperature range ²	-500	—	500	ppm
Startup time	$t_{STARTUP}$	Normal mode	—	204	—	μs
		Precision mode ¹	—	11.7	—	ms
Current consumption	I_{LFRCO}	Normal mode	—	189.9	—	nA
		Precision mode ¹ , T = stable at 25°C ³	—	649.8	—	nA

Note:

1. The LFRCO operates in high-precision mode when CFG_HIGHPRECEN is set to 1. High-precision mode is not available in EM4.
2. Includes ±40 ppm frequency tolerance of the HFXO crystal.
3. Includes periodic re-calibration against HFXO crystal oscillator.

4.14 GPIO Pins

Table 17: GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODE _x = DISABLED, VDD = 3.0 V	—	2.5	—	nA
Input low voltage ¹	V_{IL}	Any GPIO pin	—	—	0.3*VDD	V
		RESET _n	—	—	0.3*DVDD	V
Input high voltage ¹	V_{IH}	Any GPIO pin	0.7*VDD	—	—	V
		RESET _n	0.7*DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05*VDD	—	—	V
		RESET _n	0.05*DVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20mA, VDD = 3.0 V	—	—	0.2*VDD	V
Output high voltage	V_{OH}	Sourcing 20mA, VDD = 3.0 V	0.8*VDD	—	—	V
GPIO rise time	T_{GPIO_RISE}	VDD = 3.0V, C _{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
GPIO fall time	T_{GPIO_FALL}	VDD = 3.0V, C _{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
Pull up/down resistance ²	R_{PULL}	GPIO pull-up to VDD: MODE _n = DISABLE, DOUT=1. GPIO pull-down to GND: MODE _n = WIREDORPULLDOWN, DOUT = 0.	35	44	55	kΩ
		RESET _n pin pull-up to DVDD.	35	44	—	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns
RESET _n low time to ensure pin reset	T_{RESET}		100	—	—	ns

Note:

- GPIO input thresholds are proportional to the VDD pin. RESET_n input thresholds are proportional to the internal DVDD supply, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VDD when DC-DC is inactive.
- GPIO pull-ups connect to VDD supply, pull-downs connect to GND. RESET_n pull-up connects to internal DVDD supply, which is generated by the DC-DC converter. DVDD is equal to 1.8V when DC-DC is active and bypassed to VDD when DC-DC is inactive.

4.15 Microcontroller Peripherals

The MCU peripherals set available in Lyra 24P modules includes:

- ADC: 12-bit at 1 Msps, 16-bit at 76.9 ksps
- 16-bit and 32-bit Timers/Counters
- 24-bit Low Energy Timer for waveform generation
- 32-bit Real Time Counter
- USART (UART/SPI/SmartCards/IrDA/I2S)
- EUSART (UART/IrDA)
- I²C peripheral interfaces
- 12 Channel Peripheral Reflex System

For details on their electrical performance and to learn which GPIO ports provide access to every peripheral, consult the relevant portions of Section 4 and Section 6 in the SoC datasheet, see [EFR32BG24 SoC](#) section for datasheet link.

To learn which GPIO ports provide access to every peripheral, consult [Analog Peripheral Connectivity](#) and [Digital Peripheral Connectivity](#) sections.

4.16 Antenna Radiation and Efficiency for Lyra 24P Integrated Antenna

Typical performance curves indicate typical characterized performance under the stated conditions.

Typical Lyra 24P radiation patterns and efficiency for the integrated antenna under optimal operating conditions are plotted in the figures that follow. Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna.

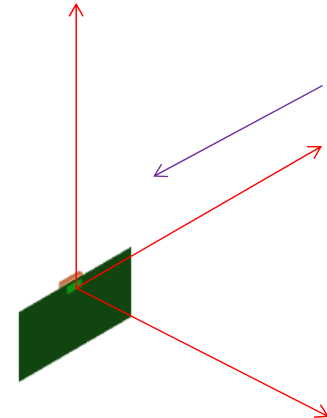
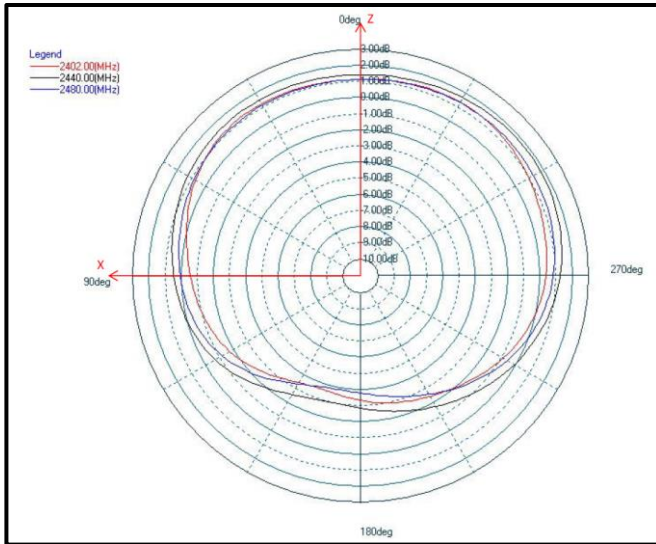


Figure 6: Lyra 24P Integrated Antenna Module Typical 2D Antenna Radiation Patterns - Phi 0° (Side View) Gain dBi

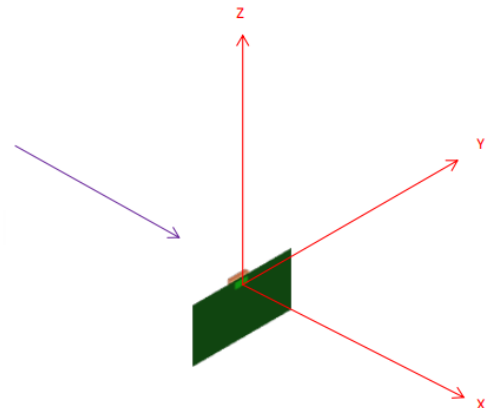
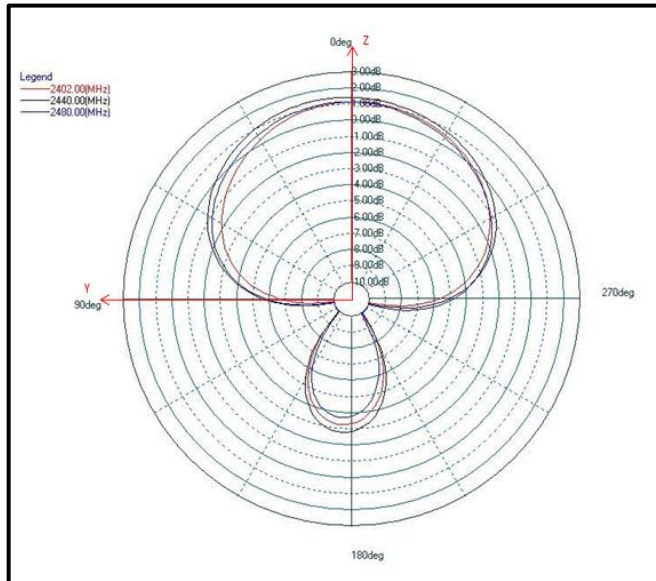


Figure 7: Lyra 24P Integrated Antenna Module Typical 2D Antenna Radiation Patterns - Phi 90° (Top View) Gain dBi

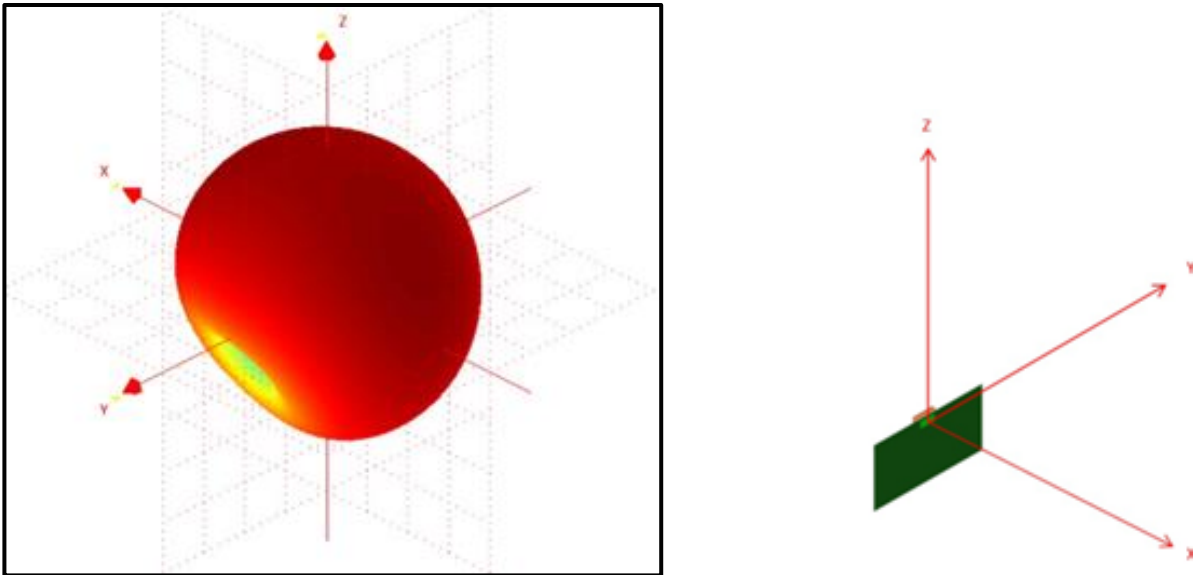


Figure 8: Lyra 24P Integrated Antenna Module Typical 2D Antenna Radiation Patterns - 3D Radiation Pattern at 2440 MHz

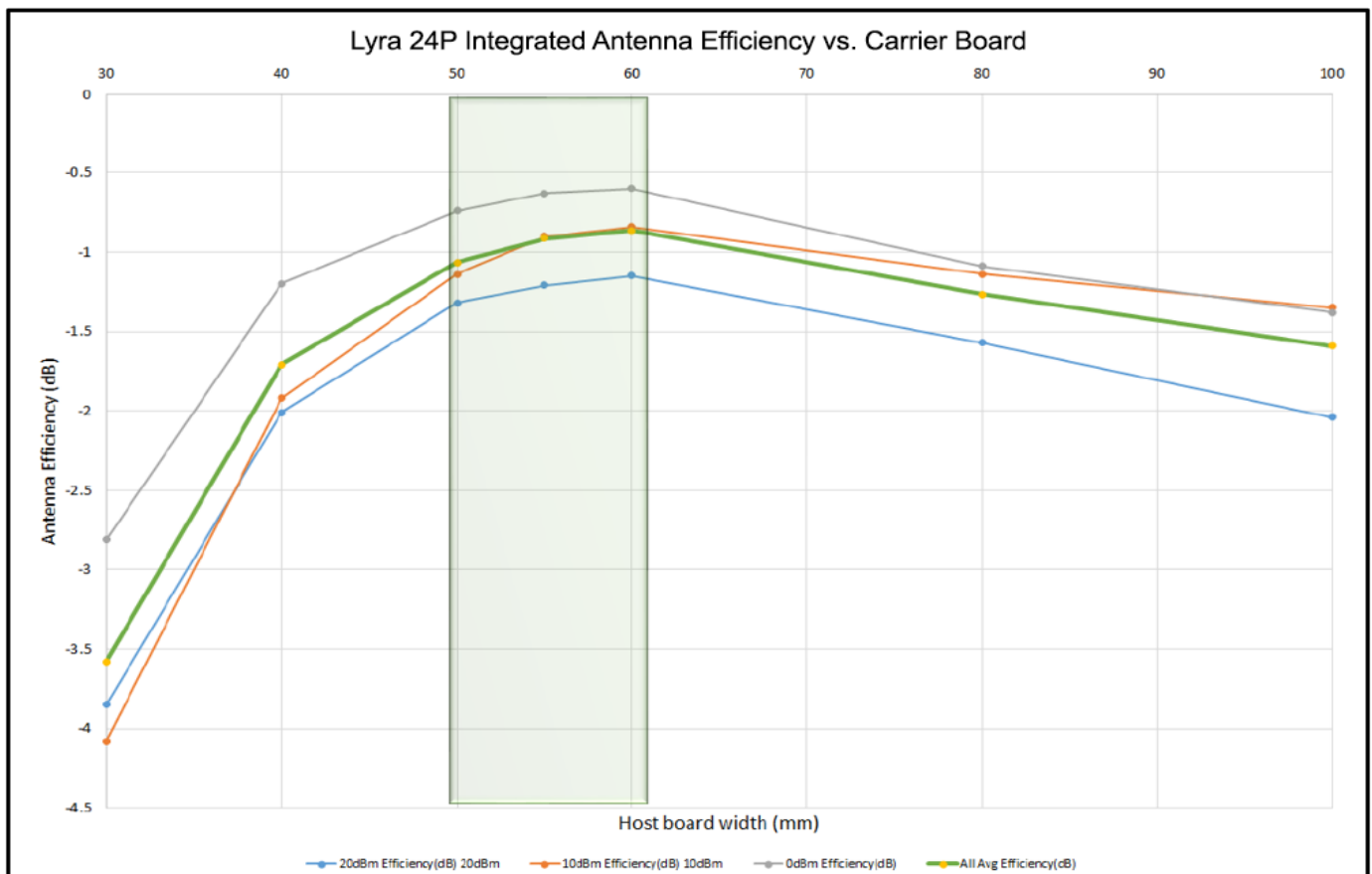


Figure 9: Radiation efficiency of the Built-in Antenna as Function of the Carrier Board Width(mm)

5 REFERENCE DIAGRAMS

5.1 Network Co-Processor (NCP) Application with UART Host

The Lyra 24P can be controlled over the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug interface, and host interface connections are shown in the figure below. For more details, see [AN958: Debugging and Programming Interfaces for Custom Designs](#).

Note: For boot pin, see section 5.3.

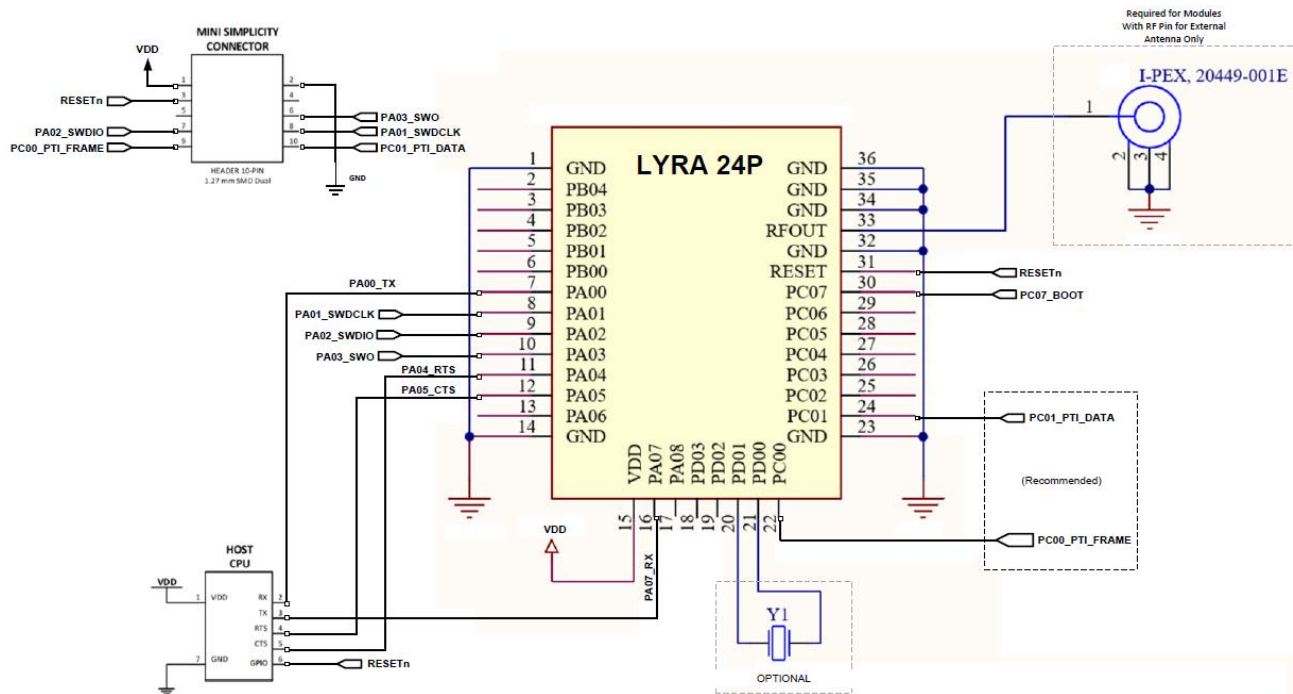


Figure 10: UART NCP Configuration (External Antenna MHF4 RF connector only required for 453-00148 Lyra 24P, RF trace pad variant module)

5.2 SoC Application

The Lyra 24P can be used in a stand-alone SoC configuration without an external host processor. Typical power supply and programming/debug interface connections are shown in the figure below. For more details, see [AN958: Debugging and Programming Interfaces for Custom Designs](#).

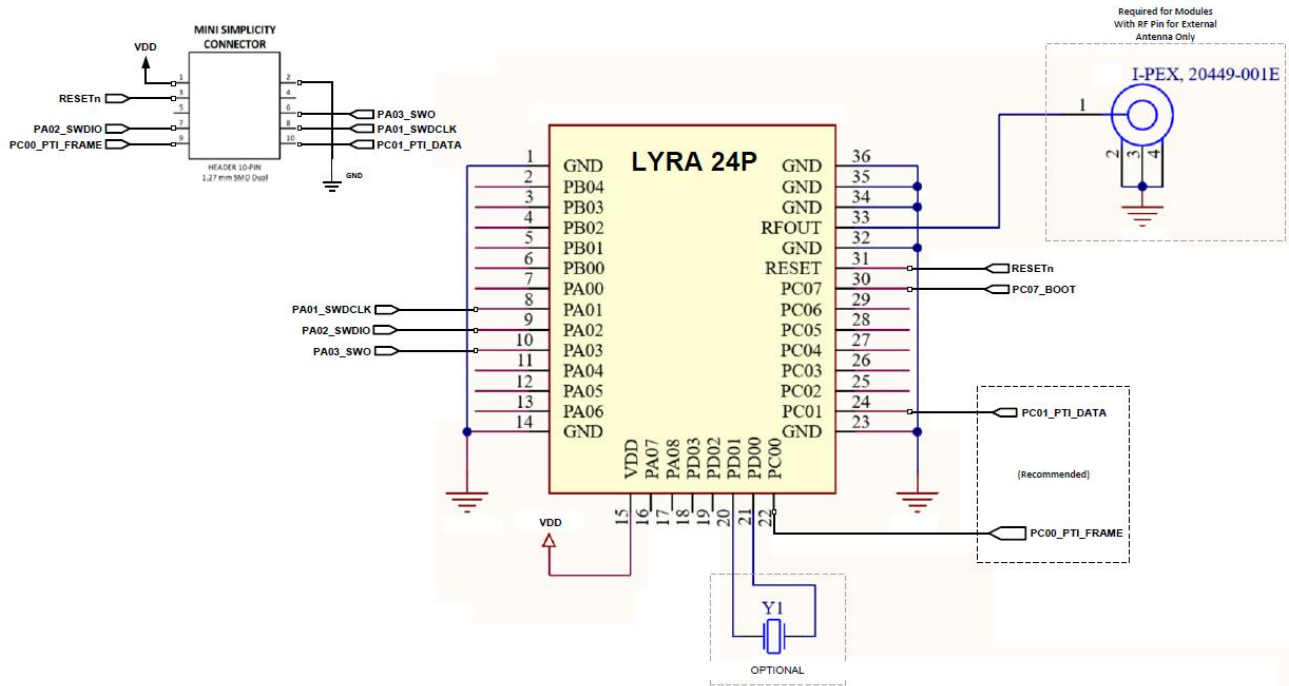


Figure 11: Stand-Alone SoC Configuration (External Antenna MHF4 RF connector only required for 453-00148 Lyra 24P, RF trace pad variant module)

5.3 Boot

The **BOOT** pin is used to determine when execution of the bootloader is required. Upon reset, execution of the bootloader begins. The **state of the BOOT pin is read immediately upon start-up of the bootloader**. If LOW, execution of the bootloader continues, facilitating firmware update via the UART. If the BOOT pin is HIGH, the bootloader will stop execution and pass control to the main application firmware.

6 PIN DEFINITIONS

6.1 Lyra 24P 36-Pin PCB Module Pinout

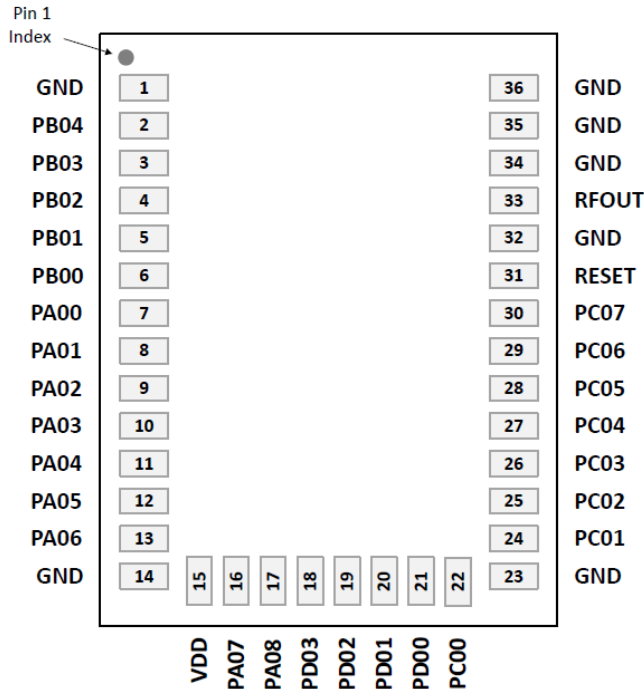


Figure 12: Lyra 24P 36-Pin PCB Module With LF Crystal Device Pinout

For GPIO pin to peripheral assignment in AT firmware, see User Guide – AT Interface Application – Lyra 24 Series.

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [Table 19: GPIO Alternate Function Table](#), [Analog Peripheral Connectivity](#), and [Digital Peripheral Connectivity](#).

Table 18: Lyra 24P Module Pin Definitions

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
GND	1	Ground	PB04	2	GPIO
PB03	3	GPIO	PB02	4	GPIO
PB01	5	GPIO	PB00	6	GPIO
PA00	7	GPIO	PA01	8	GPIO
PA02	9	GPIO	PA03	10	GPIO
PA04	11	GPIO	PA05	12	GPIO
PA06	13	GPIO	GND	14	GND
VDD	15	Power Supply	PA07	16	GPIO
PA08	17	GPIO	PD03	18	GPIO
PD02	19	GPIO	PD01	20	GPIO / LF XTAL Input (Optional)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PD00	21	GPIO / LF XTAL Output (Optional)	PC00	22	GPIO
GND	23	GPIO	PC01	24	GPIO
PC02	25	GPIO	PC03	26	GPIO
PC04	27	GPIO	PC05	28	GPIO
PC06	29	GPIO	PC07	30	GPIO
RESETn	31	Reset Pin. The RESETn pin is pulled up to an internal DVDD supply. An external pull-up is not recommended. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. The RESETn pin can be left unconnected if no external reset switch or source is used.	GND	32	GND
RFOUT	33	RF Input/Output (External Ant.)	GND	34	GND
GND	35	GND	GND	36	GND

6.2 Alternate Function Table

Some GPIOs support alternate functions like debugging, wake-up from EM4, external low frequency crystal access, etc.. The following table shows which module pins have alternate capabilities and the functions they support. Refer to the SoC's reference manual for more details.

Table 19: GPIO Alternate Function Table

GPIO	Alternate Function		
PA00	IADC0.VREFP		
PA01	GPIO.SWCLK		
PA02	GPIO.SWDIO		
PA03	GPIO.SWV	GPIO.TDO	GPIO.TRACEDATA0
PA04	GPIO.TDI	GPIO.TRACECLK	
PA05	GPIO.TRACEDATA1	GPIO.EM4WU0	
PA06	GPIO.TRACEDATA2		
PA07	GPIO.TRACEDATA3		
PB00	VDAC0.VDAC_CH0_MAIN_OUTPUT		
PB01	GPIO.EM4WU3	VDAC0.VDAC_CH_MAIN_OUTPUT	
PB02	VDAC1.VDAC_CH0_MAIN_OUTPUT		
PB03	GPIO.EM4WU4	VDAC1.VDAC_CH1_MAIN_OUTPUT	
PC00	GPIO.EM4WU6		
PC01	GPIO.EFP_TX_SDA		

GPIO	Alternate Function		
PC02	GPIO.EFP_TX_SCL		
PC05	GPIO.EFP_INT	GPIO.EM4WU7	
PC07	GPIO.EM4WU8	GPIO.THMSW_EN	GPIO.THMSW_HALFSWITCH
PD00	LFXO.LFXTAL_O		
PD01	LFXO.LFXTAL_I	LFXO.LF_EXTCLK	
PD02	GPIO.EM4WU9		

6.3 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. **When a differential connection is being used, positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins.** When a single ended connection is being used positive input is available on all pins. See the SoC's Reference Manual for more details on the ABUS and analog peripherals, [EFR32BG24 SoC](#).

Table 20: ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACMP1	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC0	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC0	VDAC_CH0_ABUS_OUTPUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	VDAC_CH1_ABUS_OUTPUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC1	VDAC_CH0_ABUS_OUTPUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	VDAC_CH1_ABUS_OUTPUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.4 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port.

Table 21: DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
ACMP1.DIGOUT			Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1	Available	Available		
CMU.CLKOUT2	Available	Available		
EUSART0.CS	Available	Available		
EUSART0.CTS	Available	Available		
EUSART0.RTS	Available	Available		
EUSART0.RX	Available	Available		
EUSART0.SCLK	Available	Available		
EUSART0.TX	Available	Available	Available	Available
EUSART1.CS	Available	Available	Available	Available
EUSART1.CTS	Available	Available	Available	Available
EUSART1.RTS	Available	Available	Available	Available
EUSART1.RX	Available	Available	Available	Available
EUSART1.SCLK	Available	Available	Available	Available
EUSART1.TX			Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT	Available	Available		
HFX00.BUFOUT_REQ_IN_ASYNC	Available	Available	Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA			Available	Available
I2C1.SCL			Available	Available
I2C1.SDA	Available	Available	Available	Available
KEYSCAN.COL_OUT_0	Available	Available	Available	Available
KEYSCAN.COL_OUT_1	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
KEYSCAN.COL_OUT_2	Available	Available	Available	Available
KEYSCAN.COL_OUT_3	Available	Available	Available	Available
KEYSCAN.COL_OUT_4				
KEYSCAN.COL_OUT_5	Available	Available	Available	Available
KEYSCAN.COL_OUT_6	Available	Available	Available	Available
KEYSCAN.COL_OUT_7	Available	Available	Available	Available
KEYSCAN.ROW_SENSE_0	Available	Available		
KEYSCAN.ROW_SENSE_1	Available	Available		
KEYSCAN.ROW_SENSE_2	Available	Available		
KEYSCAN.ROW_SENSE_3	Available	Available		
KEYSCAN.ROW_SENSE_4	Available	Available		
KEYSCAN.ROW_SENSE_5	Available	Available		
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PCNT0.S0IN	Available	Available		
PCNT0.S1IN	Available	Available		

Peripheral.Resource	PORT			
	PA	PB	PC	PD
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.ASYNCH12	Available	Available		
PRS.ASYNCH13	Available	Available		
PRS.ASYNCH14	Available	Available		
PRS.ASYNCH15	Available	Available		
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
RAC.LNAEN	Available	Available	Available	Available
RAC.PAEN	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available

7 DESIGN GUIDELINES

7.1 Layout and Placement

For optimal performance of the Lyra 24P:

Place the module aligned to the edge of the application PCB, as illustrated in the figures below.

- Optional on the module with the RF pin.
- Leave the antenna clearance area void of any traces, components, or copper on all layers of the application PCB if you are going to use the built-in antenna.
- Antenna clearance area is not necessary if you are using an external antenna attached to the RF pin.
- RFOUT can be left floating if not used.

Antennas external to the module, either connectorized off-the-shelf antennas or PCB trace antennas, must be well-matched to 50 Ω .

- For external antenna use cases, use a 50 Ω grounded coplanar transmission line to trace the signal from the RF pin to an external MHF4 RF connector if applicable (see [Figure 14](#)).
- A general rule is to use 50 Ω transmission lines where the length of the RF trace is longer than $\lambda/16$ at the fundamental frequency, which for 2.4 GHz is approximately 3.5 mm.
- An IPEX MHF4 RF connector can be used in the host PCB for the connection to an external antenna. The use of a MHF4 connector is also recommended for conductive tests. The integrator must use a unique connector, such as a “reverse polarity SMA” or “reverse thread SMA”, if detachable antenna is offered with the host chassis. This is especially required for the FCC and ISED approvals to remain valid, and any other kind of direct connector to the antenna might require a permissive change.
- A trace length of 1.84 mm was used in the certifications host board to connect the module RF pin to the MHF4 RF connector.
- For reference, [Figure 18](#) shows a set of parameters for a 50 Ω trace. Trace impedance should always be matched to the particular stack-up used on the host board.

Connect all ground pads directly to a solid ground plane.

Place the ground vias as close to the ground pads as possible.

Avoid plastic or any other dielectric material in contact with the antenna.

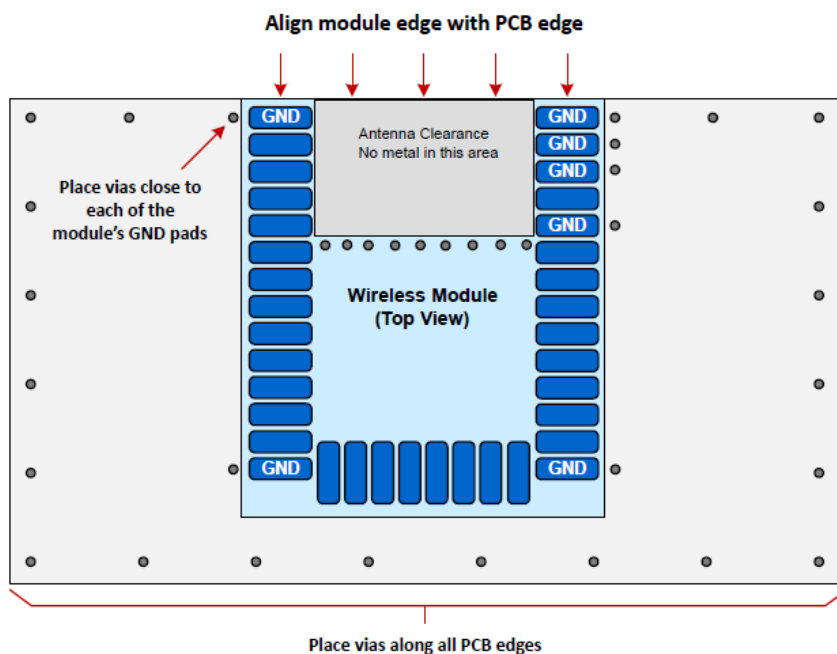


Figure 13: Recommended Layout for Lyra 24P Using Built-in Antenna

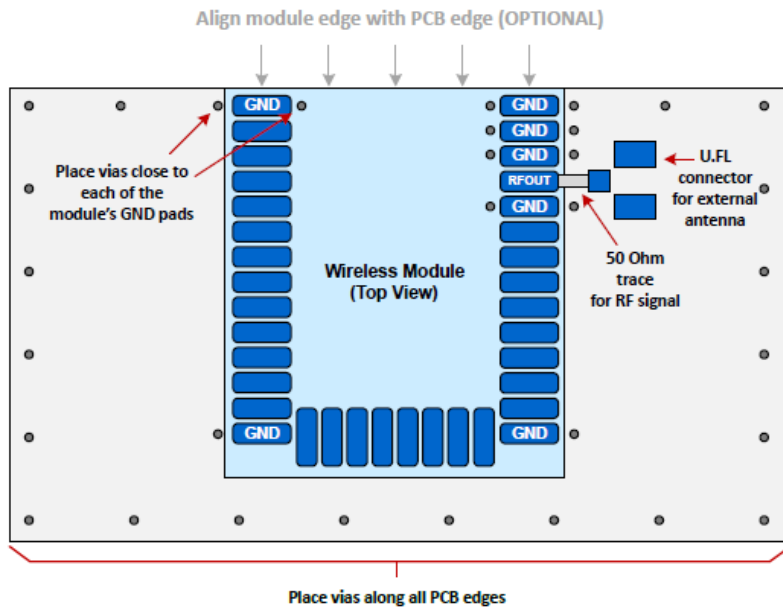


Figure 14: Recommended Layout for Lyra 24P Using External Antenna

The figure below illustrates layout scenarios that will lead to severely degraded RF performance for the module.

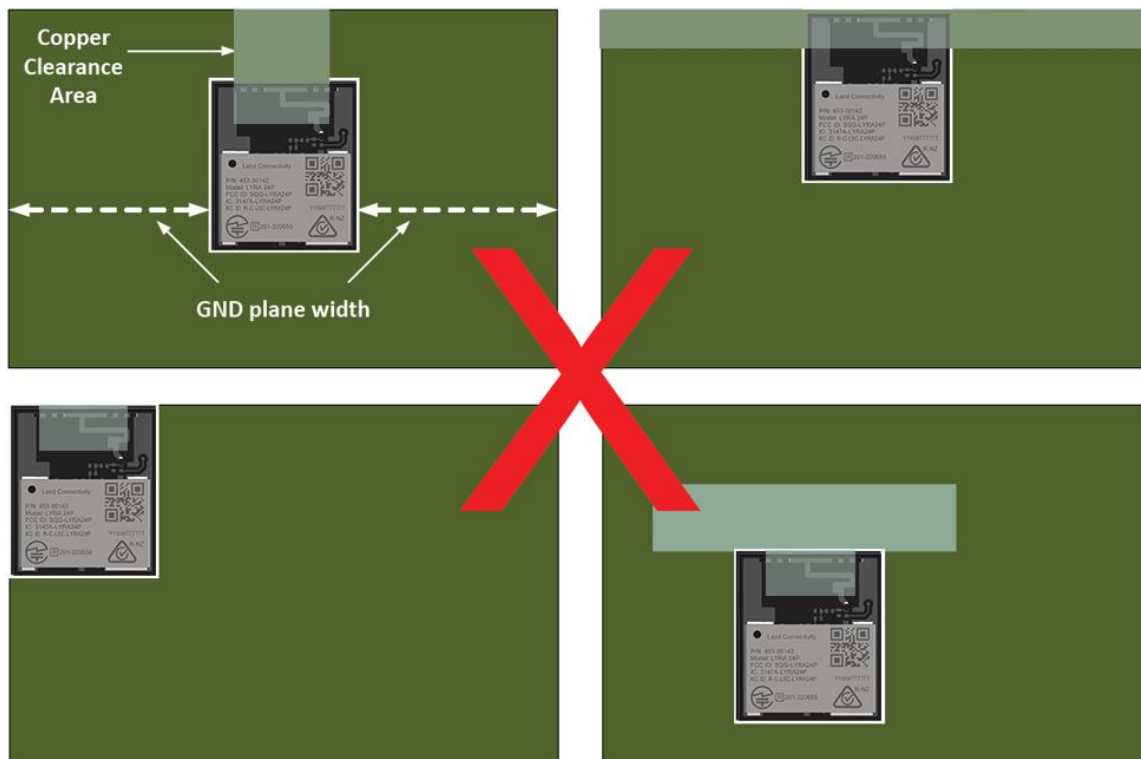


Figure 15: Non-optimal layout examples

The width of the GND plane to the sides the module will impact the efficiency of the built in antenna. **To achieve optimal performance, a GND plane width of 55-60 mm is recommended.** See [Antenna Radiation and Efficiency](#) for reference.

7.2 Proximity to Other Materials

Avoid plastic or any other dielectric material in close contact with the antenna. Conformal coating and other thin dielectric layers are acceptable directly on top of the antenna region, but this will also negatively impact antenna efficiency and reduce range.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

7.3 Proximity to Human Body

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.

7.4 Reset

The Lyra 24P can be reset by pulling the RESET line low, by the internal watchdog timer, or by software command.

The reset state does not provide power saving functionality and it is not recommended as a means to conserve power.

7.5 Debug

The Lyra 24P supports hardware debugging via 4-pin JTAG or 2-pin serial-wire debug (SWD) interfaces. **It is recommended to expose the debug pins in your own hardware design for firmware update and debug purposes.** The table below lists the required pins for JTAG and SWD debug interfacing, which are also presented in Section [Alternate Function Table](#).

If JTAG interfacing is enabled, the module must be power cycled to return to a SWD debug configuration if necessary.

Table 22: Debug Pins

Pin Name	JTAG Signal	SWD Signal	Comments
PA04	TDI	N/A	This pin is disabled after reset. Once enabled the pin has a built-in pull-up.
PA03	TDO	N/A	This pin is disabled after reset.
PA02	TMS	SWDIO	Pin is enabled after reset and has a built-in pull-up.
PA01	TCK	SWCLK	Pin is enabled after reset and has a built-in pull-down.

7.6 Packet Trace Interface (PTI)

The Lyra 24P integrates a true PHY-level packet trace interface (PTI) peripheral that can capture packets non-intrusively to monitor and log device and network traffic without burdening processing resources in the module's SoC. The PTI generates two output signals that can serve as a powerful debugging tool, especially in conjunction with other hardware and software development tools available from Silicon Labs. The **PTI_DATA** and **PTI_FRAME** signals can be accessed through any GPIO on ports C and D (see **FRC.DOUT** and **FRC.DFRAME** peripheral resources in [Pin Definitions](#)).

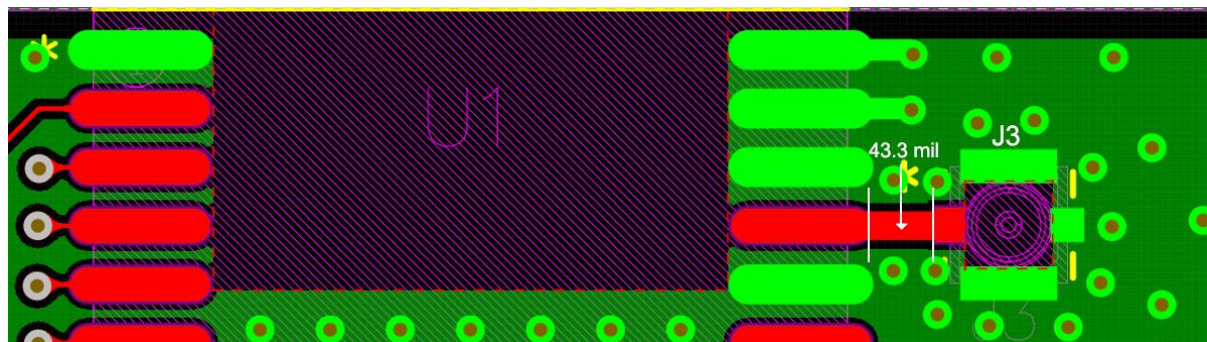
7.7 Lyra 24P Module 50 Ohms RF Track Design for Connecting External Antenna with the Lyra 24P Module, 20dBm, RF Pad Variant (453-00148)

Lyra 24P module can be used with external antennas (certified by Laird Connectivity), and requires a 50 Ohm RF trace (GCPW, that Grounded Coplanar Waveguide) to be designed to run from Lyra 24P module RFOUT (pin33) to a RF antenna connector (IPEX MHF4) on host PCB. The **50 Ohms RF track design and length MUST be copied** (as specified in this section). Lyra 24P module GND pin32 and GND pin34 used to support GCPW 50Ohm RF trace.

Checklist for SCH

Lyra 24P External antenna connection SCH	Lyra 24P External antenna connection PCB
<p>1. Fit IPEX MHF4 RF connector (20449-001E)</p>	

Figure 16: Lyra 24P for External antenna connection host PCB 50-Ohm RF trace schematic with MHF4 RF connector Layer1 (RF Track and RF GND)



Layer2 (RF GND)

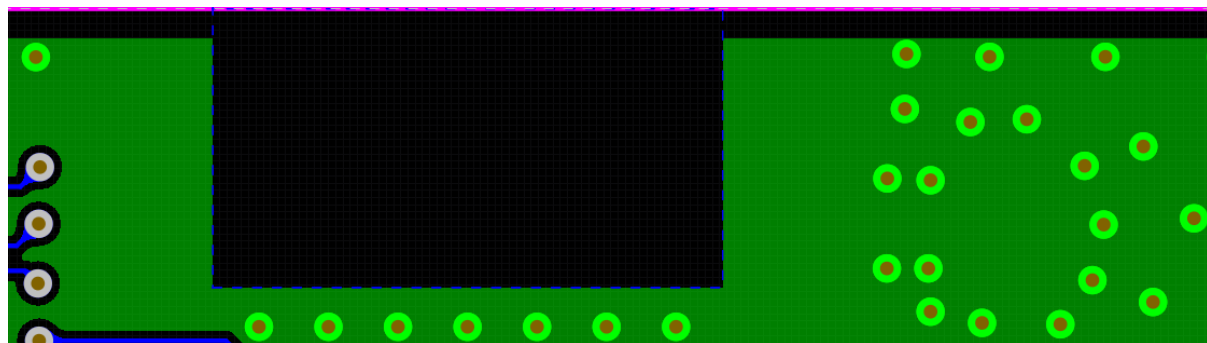
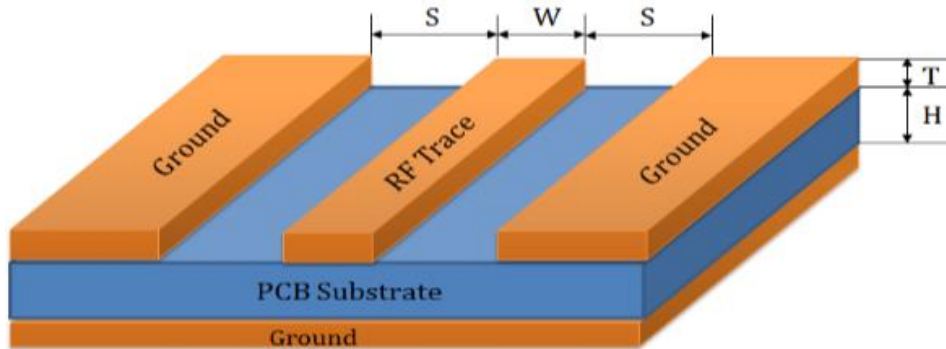


Figure 17: 50-Ohm RF trace design (Layer1 and Layer2) on DVK-Lyra 24P development board 453-00148-K1 (or host PCB) for use with Lyra 24P (453-00148) module

Checklist for PCB:

- MUST use a 50-Ohm RF trace (GCPW, that is Grounded Coplanar Waveguide) from RFOUT pad (pin33) of the Lyra 24P module (453-00148) to RF antenna connector (IPEX MHF4 Receptable (MPN: 20449-001E)) on host PCB.
- To ensure regulatory compliance, MUST follow exactly the following considerations for 50-Ohms RF trace design and test verification:



	Thickness		Dielectric	
	mil	mm	Constant Er	
Solder Mask	1.0	0.025	3.5	Stack up for 50 Ohms GCPW RF Track.
Layer1 Copper 1oz+plating	1.5	0.038		
Core	57.60	1.463	4.2	
Layer2 Copper 1oz+plating	1.5	0.038		
Solder Mask	1.0	0.025	3.5	
Total	62.6	1.59		

Figure 18: Lyra 24P development board PCB stack-up and 50-Ohms Grounded CPW RF trace design using GND on L1 and L2

Note 1: The plating (ENIG) above base 1ounce copper is not listed, but plating expected to be ENIG.

- The 50-Ohms RF trace design MUST be Grounded Coplanar Waveguide (GCPW) with
 - Layer1 RF track width (W) of 20 mil and
 - Layer1 gap (S) to GND of 5 mil and where the
 - Layer1 to Layer 2 dielectric thickness (H) MUST be 57.6 mil (dielectric constant Er 4.2).
 - Further the Layer1 base copper must be 1-ounce base copper (that is 1.5 mil) plus the plating and
 - Layer1 MUST be covered by solder mask of 1.0 mil thickness (dielectric constant Er 3.5).
- The 50-Ohms RF trace design MUST follow the PCB stack-up shown in Figure 18. (Layer1 to Layer2 thickness MUST be identical to the Lyra 24P development board).
- The 50-Ohms RF trace should be a controlled-impedance trace e.g., ±10%.
- The 50-Ohms RF trace length MUST be identical (as seen in Figure 17) (43.3mil) to that on the Lyra 24P development board from Lyra 24P module RFOUT RF pad (pin33) to the RF connector IPEX MHF4 Receptable (MPN: 20449-001E).
- Place GND vias regularly spaced either side of 50-Ohms RF trace to form GCPW (Grounded coplanar waveguide) transmission line as shown in Figure 17 and use Lyra 24P module GND pin32, GND pin34.
- Use spectrum analyzer to confirm the radiated (and conducted) signal is within the certification limit.

7.8 External Antenna Integration with the Lyra 24P Module, 20dBm, RF pad variant (453-00148)

Please refer to the Lyra 24P Regulatory Information Guide (coming soon) for details on using Lyra 24P module with external antennas in each regulatory region. This guide will be available at: www.lairdconnect.com/lyra24-series.

The Lyra 24P has been designed to operate with the below external antennas (with a maximum gain of 2.0dBi). The required antenna impedance is 50 ohms. See [Table 23](#). External antennas improve radiation efficiency.

Table 23 : External antennas for the Lyra 24P

Manufacturer	Model	Laird Connectivity Part Number	Weight	Dimensions	Type	Connector	Peak Gain	
							2400-2500 MHz	2400-2480 MHz
Laird Connectivity	NanoBlue	EBL2400A1-10MH4L		44.45mm x 12.7mm x 0.81 mm	PCB Dipole	IPEX MHF4	2 dBi	-
Laird Connectivity	FlexPIFA	001-0022	1.13g	40.1mm x 11.0mm x 2.5mm	PIFA	IPEX MHF4	-	2 dBi
Mag Layers	EDA-8709-2G4C1-B27-CY	0600-00057	NA	NA	Dipole	IPEX MHF4	2 dBi	-
Laird Connectivity	mFlexPIFA	EFA2400A3S-10MH4L	1.8g	25.4 mm x 23.4 mm x 2.5 mm	PIFA	IPEX MHF4	-	2 dBi

8 MECHANICAL SPECIFICATIONS

8.1 Dimensions (Lyra 24P series modules)

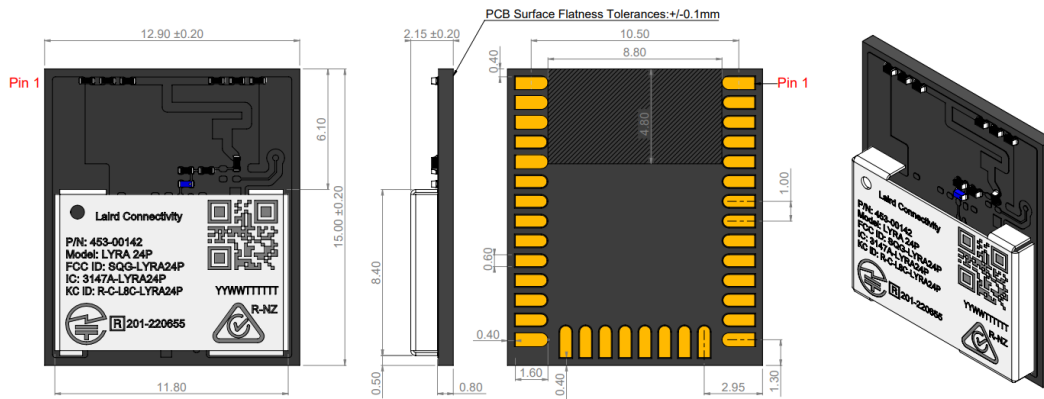


Figure 19: LYRA 24P +10 dBm Module dimensions (mm)

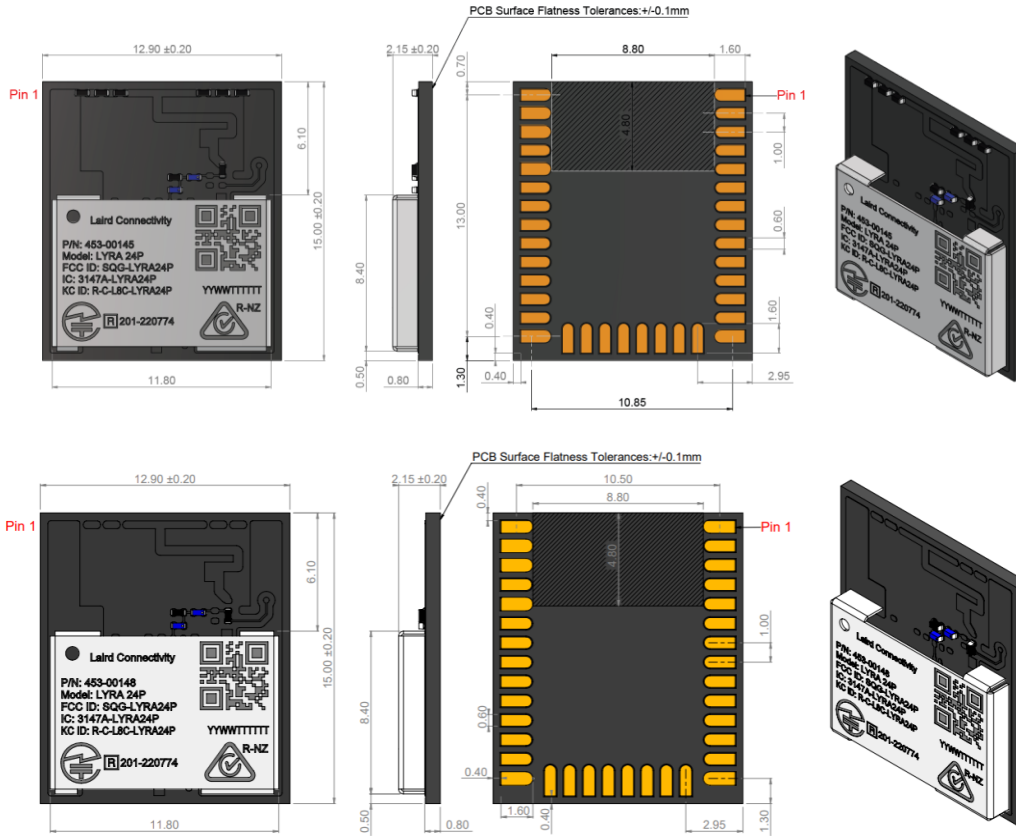


Figure 20: LYRA 24P +20 dBm Module, Integrated Antenna (453-00145) and LYRA 24P +20 dBm Module, RF Trace pad variant (453-00148) dimensions (mm)

8.2 PCB Land Pattern (Lyra 24P series modules)

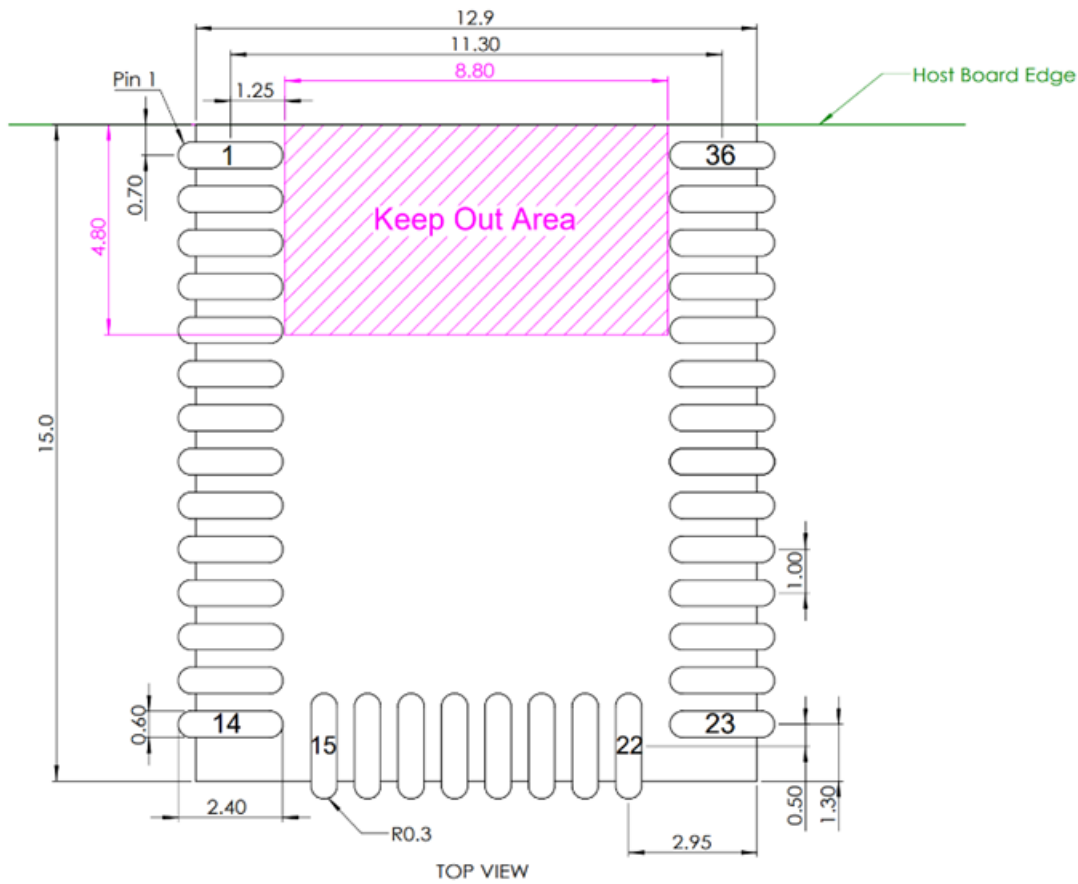


Figure 21: PCB land pattern

Note: For modules with RF pin, the antenna keep out zone in the PCB land pattern above should be omitted.

8.3 Dimensions for 450-00184 Lyra 24P – Bluetooth v5.4 USB Adaptor (20dBm) with Integrated Antenna (Silicon Labs EFR32BG24)

The Lyra 24P USB dongle User Guide is available on the Lyra 24 Series product page:

<https://www.lairdconnect.com/lyra24-series>

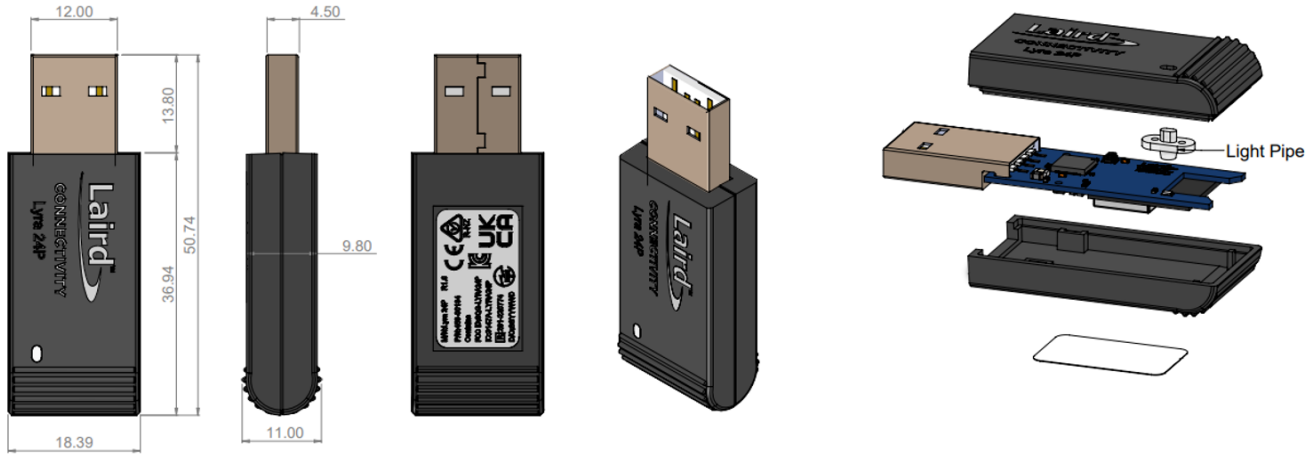


Figure 22: Lyra 24P USB Module - Dimensions

8.4 Lyra 24P Series Module Label Marking

The figure below shows the module markings engraved on the RF shield.

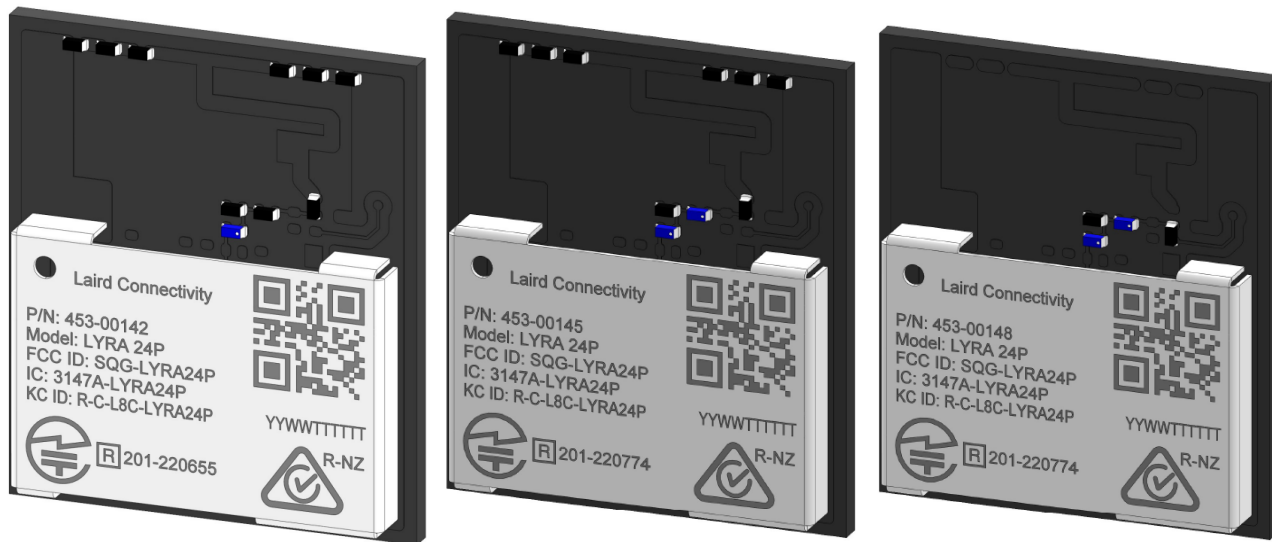


Figure 23: Lyra 24P Top Marking – +10dBm (Integrated antenna), +20 dBm (integrated antenna) and +20 dBm (RF pad) Modules Shown

Mark Description

The package marking consists of:

- P/N - Part number designation
- Model: Lyra 24P Model number designation
- QR Code: YYWWTTTTTT
 - YY – Last two digits of the assembly year.
 - WW – Two-digit workweek when the device was assembled.
 - TTTTTT – Manufacturing trace code. The first two letters are the ID of the manufacturer followed by 4 digits of trace code.
- Date code: YYWWTTTTTT
 - YY – Last two digits of the assembly year.
 - WW – Two-digit workweek when the device was assembled.
 - TTTTTT – Manufacturing trace code. The first two letters are the ID of the manufacturer followed by 4 digits of trace code.
- Certification marks such as the CE logo, FCC, and IC IDs, etc as per above image.

8.5 Lyra 24P USB Adapter Label Marking



Figure 24: Lyra 24P USB Adapter Label Marking

Mark Description

The package marking consists of:

- P/N - Part number designation
- Model: Lyra 24P Model number designation
- Date Code: YYWWTTTTTTT
 - YY – Last two digits of the assembly year.
 - WW – Two-digit workweek when the device was assembled.
 - TTTTTT – Manufacturing trace code. The first two letters are the ID of the manufacturer followed by 4 digits of trace code.
- Certification marks such as the CE logo, FCC, and IC IDs, etc as per above image.

8.6 Lyra 24P USB Adapter Antenna Radiation Pattern

The Lyra 24P USB adaptor uses the 453-000145 - Lyra 24P Series - Bluetooth v5.4 PCB Module (20dBm) with integrated antenna module which has 1.82dBi antenna gain.

The Lyra 24P USB adaptor small PCB size (small ground plane) limits the radiated antenna performance. See Lyra 24P USB adaptor antenna patterns in X, Y and Z orientations for 3 channels.

Table 24: Lyra 24P USB Adapter antenna gain (X, Y, and Z planes)

Antenna Gain in dBi	2402MHz		2440MHz		2480MHz	
	Peak	Average	Peak	Average	Peak	Average
X plane Azimuth	-5.72dBi	-8.22dBi	-4.82dBi	-7.02dBi	-4.56dBi	-6.82dBi
X plane Elevation	-22.71dBi	-27.82dBi	-21.38dBi	-27.04dBi	-21.06dBi	-26.77dBi
Y plane Azimuth	-17.24dBi	-22.9dBi	-16.11 dBi	-20.98dBi	-16.69dBi	-21.09dBi
Y plane Elevation	-6.1dBi	-8.68dBi	-4.83dBi	7.27dBi	-4.08dBi	-6.54dBi
Z plane Azimuth	-7.36dBi	-12.78dBi	-6.07dBi	-11.62dBi	-5.61dBi	-11.18dBi
Z plane Elevation	-6.48dBi	-10.82dBi	-4.79dBi	-9.47dBi	-4.21dBi	-8.93dBi

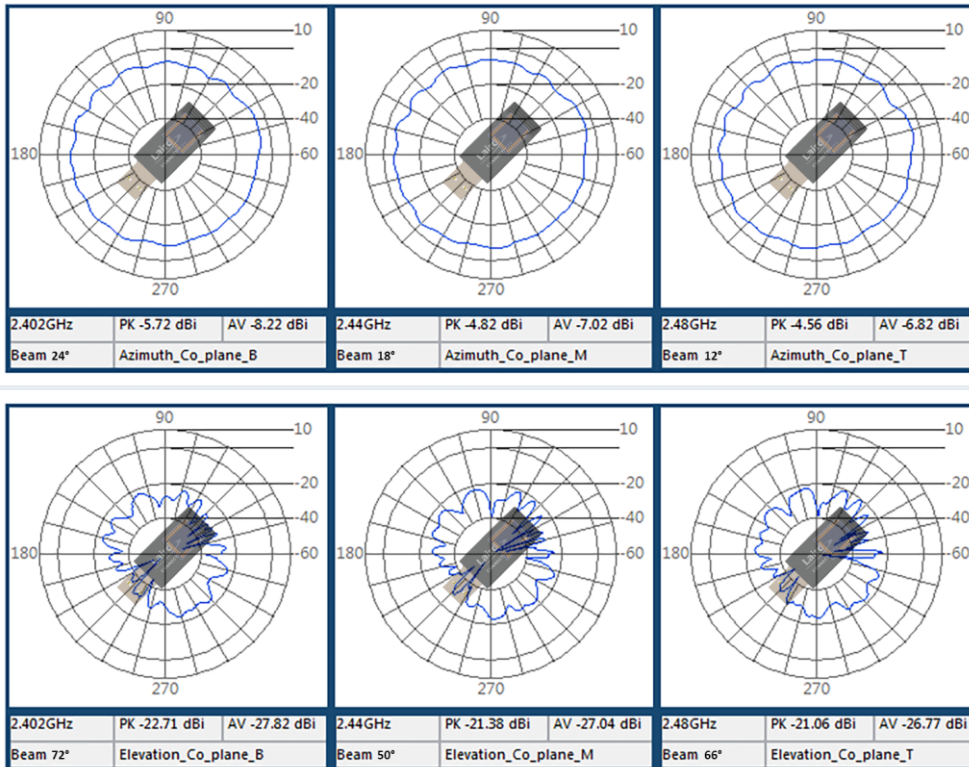


Figure 25: X-Plane Antenna Radiation Pattern

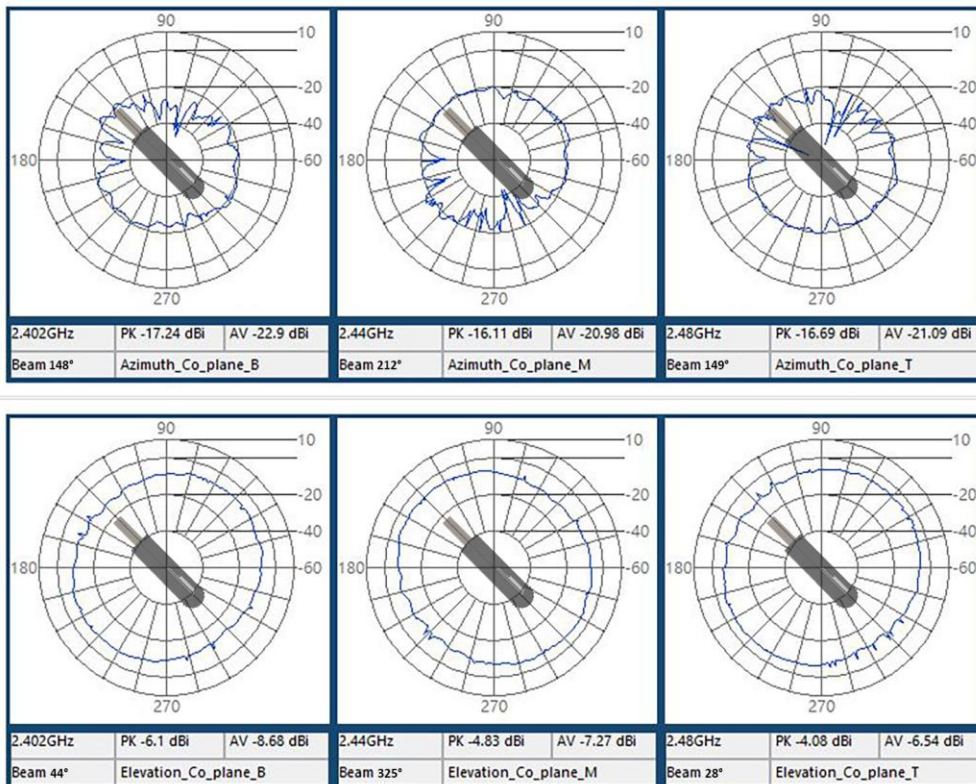


Figure 26: Y-Plane Antenna Radiation Pattern

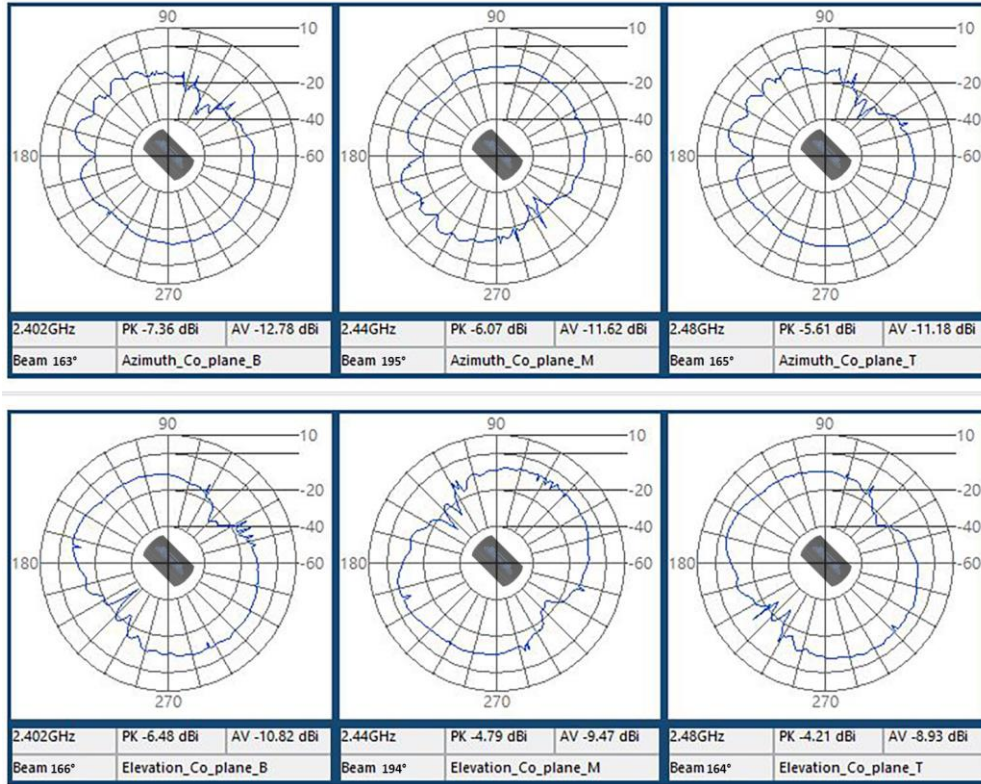


Figure 27: Z-Plane Antenna Radiation Pattern

9 SOLDERING RECOMMENDATIONS

9.1 Reflow for lead Free Solder Paste

- Optimal solder reflow profile depends on solder paste properties and should be optimized as part of an overall process development.
- It is important to provide a solder reflow profile that matches the solder paste supplier's recommendations.
- Temperature ranges beyond that of the solder paste supplier's recommendation could result in poor solderability.
- All solder paste suppliers recommend an ideal reflow profile to give the best solderability.

9.2 Recommended Reflow Profile for lead Free Solder Paste

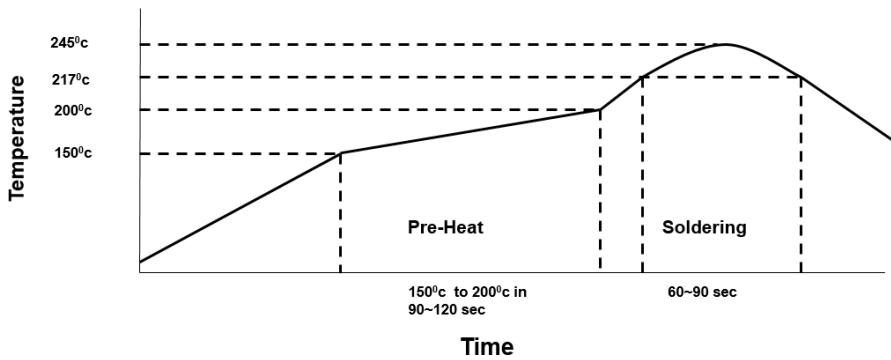


Figure 28: Recommended Reflow Profile

10 MISCELLANEOUS

10.1 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently.

10.2 Rework

The Lyra 24P module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

Never attempt a rework on the module itself, i.e. replacing individual components. Such actions terminate warranty coverage.

10.3 Handling and Storage

10.3.1 Handling

The Lyra 24P module contains a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently.

10.3.2 Moisture Sensitivity Level (MSL)

Per J-STD-020, devices rated as MSL 4 and not stored in a sealed bag with desiccant pack should be baked prior to use.

Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

10.3.3 Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40°C and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl₂, H₂S, NH₃, SO₂, or NO_x. Do not store in direct sunlight.

The product should not be subject to excessive mechanical shock.

10.3.4 Repeated Reflow Soldering

Only a single reflow soldering process is encouraged for host boards.

11 TAPE AND REEL

Lyra 24P modules are delivered to the customer in cut tape (250 pcs) or reel (1000 pcs) packaging with the dimensions below. All dimensions are given in mm unless otherwise indicated.

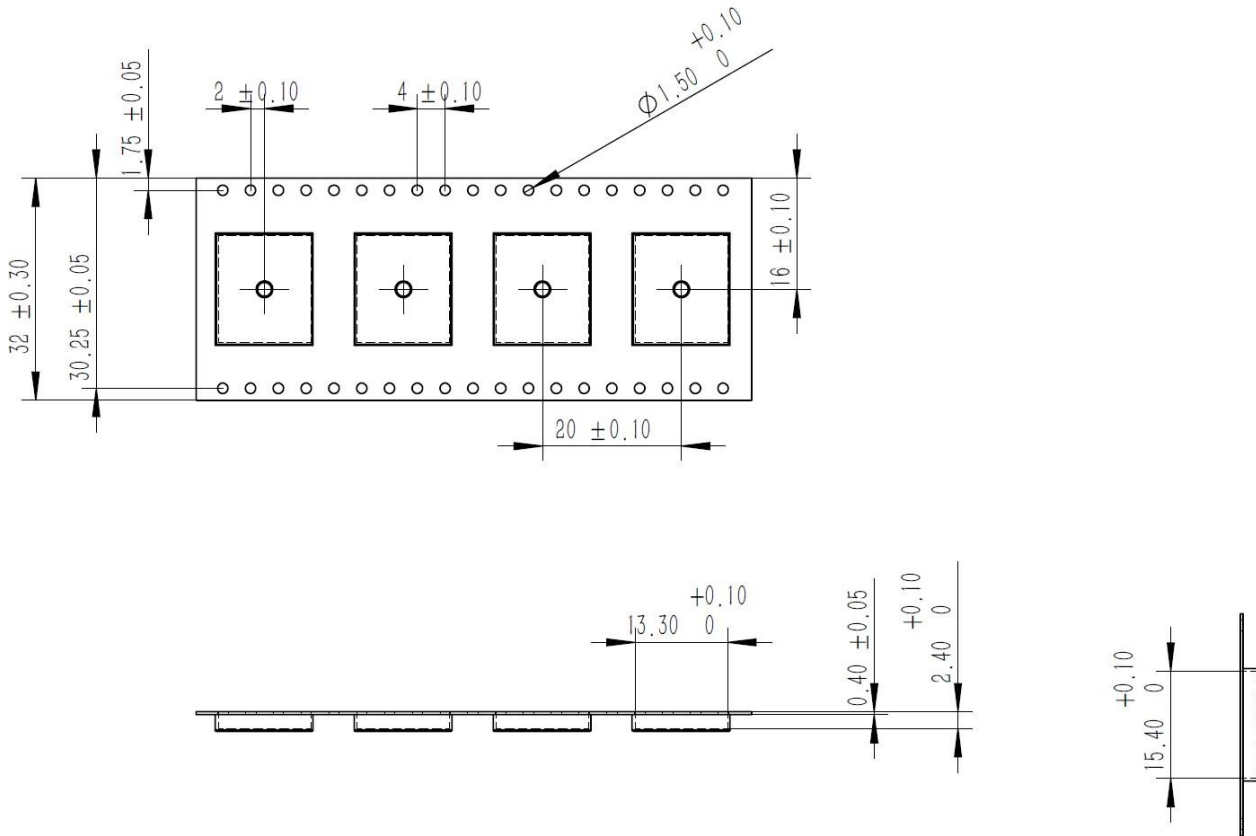


Figure 29: Carrier Tape Dimensions

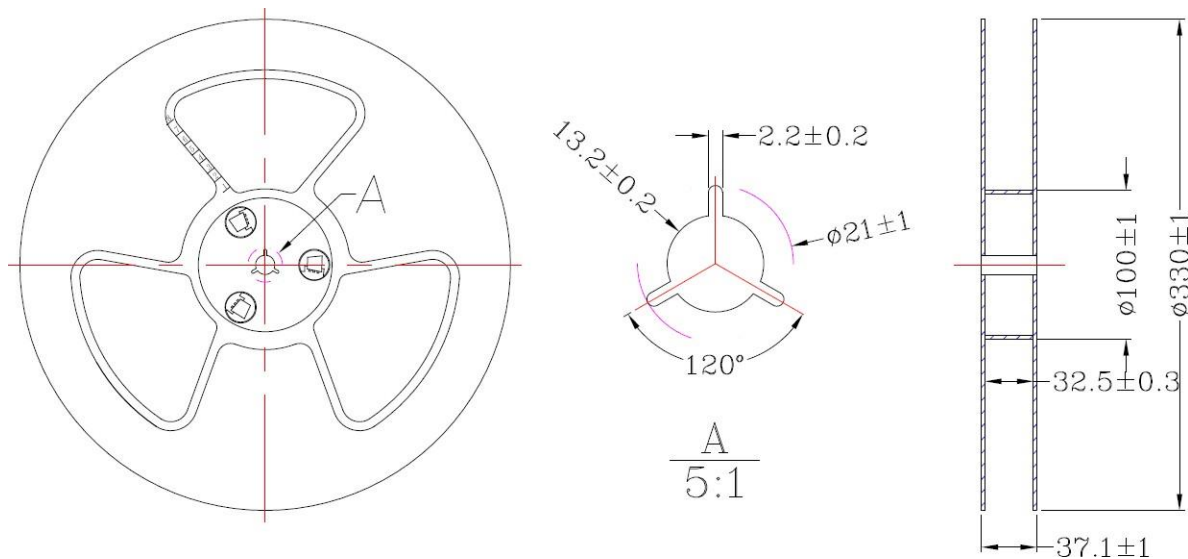


Figure 30: Reel Dimensions

12 RELIABILITY TEST

12.1 Climatic And Dynamic

Table 25: Climatic and Dynamic Reliability Test Results for Lyra 24P Modules

Test Item	Specification	Standard	Test Result
Step 1: Pre-conditioning	Pre-check:		
	1. Function check (Tools and SOP supplied by customers).		
	2. Mechanical check.		
	Pre-conditioning:		
	1. Bake: 125°C for 24 hours.		
	2. Moisture Soak: 30°C/60% RH for 192 hours		
	3. Not shorter than 15 minutes and not longer than 4 hours after removal from the temperature/humidity chamber, subject the sample to 3 cycles of the reflow.	JESD22-A113	Pass
	Post-check:		
Step 2: Temperature Cycling Non-operating	4. Function check (Tools and SOP supplied by customers).		
	5. Mechanical check.		
	6. Perform inspections of short, open, delamination of DUTs by Optical Microscope (under 40X optical magnification).		
	7. X-RAY / CSAM (SAT) on any failed samples (Notify customers).		
	8. Cross-sections analysis based on X-RAY and CSAM results.		
Step 2: Temperature Cycling Non-operating	9. Dwell on -40°C for 15 minutes		
	10. Shock to 85°C within ramp rate 15 °C/minute		
	11. Dwell on 85°C for 15 minutes	JESD22-A113	Pass
	12. Shock to -40°C within ramp rate 15 degree C/minute		
Mechanical Shock Non-operating Unpackaged device	13. Repeat step 1-4 and stop to check functions at 500/ 700 cycles		
	1. Pulse shape: Half-sine waveform		
	2. Impact acceleration: 1500 g		
	3. Pulse duration: 0.5 ms	JEDEC 22-B110B.01 (2019)	Pass
	4. Number of shocks: 30 shocks (5 shocks for each face)		
	5. Orientation: Bottom, top, left, right, front, and rear faces		

Table 26: Climatic and Dynamic Reliability Test Results for Lyra 24P USB Adapter

Test Item	Specification	Standard	Test Result
Thermal Shock	<ol style="list-style-type: none"> 1. Temperature: -40 ~ 85°C 2. Ramp time: Less than 10 seconds. 3. Dwell Time: 10 minutes 4. Number of Cycles: 500 times 	<p>*JESD22-A106 *IEC 60068-2-14 for dwell time and number of cycles</p>	Pass
Vibration Non-operating Unpackaged device	<ol style="list-style-type: none"> 1. Vibration Wave Form: Sine Waveform 2. Vibration frequency / Displacement: 20-80 Hz/1.5mm 3. Vibration frequency / Acceleration: 80-2000 Hz/20g 4. Cycle Time: 4 min/cycle 5. Number of Cycles: 4 cycle/axis 6. Vibration Axes : X, Y and Z (Rotate each axis on vertical vibration table) 	JEDEC 22-B103B (2016)	Pass
Mechanical Shock Non-operating Unpackaged device	<ol style="list-style-type: none"> 1. Pulse shape: Half-sine waveform 2. Impact acceleration: 1500 g 3. Pulse duration: 0.5 ms 4. Number of shocks: 30 shocks (5 shocks for each face) 5. Orientation: Bottom, top, left, right, front and rear faces 	JEDEC 22-B110B.01 (2019)	Pass

12.2 Reliability MTBF Prediction

Table 27: MTBF Prediction for Lyra 24P Modules

Laird Part Number	Environment	Test Result 40 °C (Hours)
453-00142R	Ground, Fixed, Uncontrolled	17,000,000
453-00142C		
453-00145R		
453-00145C		
453-00148R		
453-00148C		

Laird Part Number	Environment	Test Result 105 °C (Hours)
453-00142R	Ground, Fixed, Uncontrolled	900,000
453-00142C		
453-00145R		
453-00145C		
453-00148R		
453-00148C		

Table 28: MTBF Prediction for Lyra 24P USB Adapter

Laird Part Number	Environment	Test Result 40 °C (Hours)
450-00184	Ground, Fixed, Uncontrolled	1,311,381.23
	Ground, Mobile	2,608,428.88

Laird Part Number	Environment	Test Result 85 °C (Hours)
450-00184	Ground, Fixed, Uncontrolled	148,641.17
	Ground, Mobile	279,361.02

13 REGULATORY

13.1 Regulatory information

Note: For complete regulatory information, refer to the Lyra 24P Regulatory Information document (coming soon) which will be available from the [Lyra 24 Series Bluetooth 5.4 Solution Product page](#).

The Lyra 24P holds current certifications in the following countries:

Table 29: Lyra 24P Regulatory Information

Country/Region	Regulatory ID
USA (FCC)	SQG-LYRA24P
Canada (ISED)	3147A-LYRA24P
UK (UKCA)	N/A
EU	N/A
Japan (MIC)	201-220655 (+10 dBm) / 201-220774 (+20 dBm)
Korea (KC)	R-C-L8C-LYRA24P (Module) R-C-L8C-LYRA24PUSB (USB Adapter)
Australia (AS)	N/A
New Zealand (NZS)	N/A

13.2 Maximum Regulatory Certified RF TX Power per Country – 453-00148 Lyra 24P Series - Bluetooth v5.4 PCB Module (20dBm) with RF Trace Pad

13.2.1 For shipped AT firmware

AT firmware implements RF TX power settings per country highlighted in below table and per country sections have detailed information.

	Country and implementation	Global	EU	UK	USA	Canada	Australia	New Zealand	Japan	South Korea
AT FW	Region code	GL	EU	UK	US	CA	AU	NZ	JP	SK
AFH FW module?	Turned on or off	on	on	on	on	on	on	on	on	on
20dBm mode (>15 BLE channels free)	Target TX power conducted	17dBm	17dBm	17dBm	17dBm	17dBm	17dBm	17dBm	17dBm	17dBm
	Antenna Gain setting.	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi
	TX power setting	20dBm	20dBm	20dBm	20dBm	20dBm	20dBm	20dBm	20dBm	20dBm
	Turn off CH39 2480MHz	yes	no	no	yes	yes	no	no	no	no
10dBm mode (<15 BLE channels free)	Target TX power conducted	7dBm	7dBm	7dBm	7dBm	7dBm	7dBm	7dBm	7dBm	7dBm
	Antenna Gain setting.	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi
	TX power setting	10dBm	10dBm	10dBm	10dBm	10dBm	10dBm	10dBm	10dBm	10dBm

453-00148 Lyra 24P – Bluetooth v5.4 PCB Module (20dBm) with RF Trace Pad is shipped with AT firmware where the radio regulatory region “global” is set which is lowest common settings across RF TX power across certified countries.

To switch to the specific radio regulatory region country of USA, Canada, Europe, UK, Australia, New Zealand, Japan, and South Korea, customer can use appropriate AT command for setting the radio regulatory region per country.

13.2.2 For customers C code development

Customers developing with **C Code** – Full software development with Silicon Labs SDK and Toolchain, MUST implement the RF TX power settings per country and other parameters mentioned in this section.

13.2.3 AFH firmware module

- 1) For BLE 20dBm modules, and whenever for radio regulatory declared radio as FHSS, the Silabs AFH FW module MUST be enabled. See Silabs AFH firmware module (in Silabs BLE stack) operation description: <https://docs.silabs.com/bluetooth/5.0/general/system-and-performance/adaptive-frequency-hopping>

Below is basic summary:

- a. Does spectral scanning every one second (takes about 10ms to scan 40 BLE channels) AFTER first transmission (after an advertisement is sent)
- b. If RF interference is present on a channel (above -71dBm), then that channel is **NOT** used and is blacklisted for at least 8 afh_scan_intervals
- c. You are allowed to use TX power above +10 dBm when AFH is enabled and at least 15 channels are available
- d. Note that high transmit power is only allowed once for each channel after a measurement on that channel occurs. In other words, if you use the same channel multiple times for transmitting within afh_scan_interval, the second and consecutive transmission will use +10 dBm. If you have a short connection interval and long afh_scan_interval, this can easily happen,

- e. Other limitations:
 - “When AFH is applied, the length of the connection events (not to be confused with the connection interval) is limited to 40 ms. In other words, in every connection interval you can send packets only for 40 ms. This is usually not a problem because it takes around 2.5 ms to transmit a packet with 251B payload. However, to achieve maximum throughput with unacknowledged data transmission (see Throughput with Bluetooth Low Energy, you have to take into account this limitation. For example, if you have 100 ms connection interval, you can send packets only 40% of the time. To achieve maximum throughput, decrease your connection interval to 40 ms or lower.”
- 2) AFH FW module has high 20dBm mode and lower 10dBm mode (in both cases actual RF TX power is lower as per Laird Connectivity certified tables).
- 3) AFH FW module uses high (20dBm) mode when at least 15 BLE channels are available.
- 4) AFH FW module uses low (10dBm) mode If the number of available BLE channels are less than 15. E.g. when using legacy BLE Advert (which has only 3 BLE channels namely 2402, 2440, 2480MHz), then the AFH FW module drops to 10dBm mode.
NOTE: In both cases actual RF TX power is lower as per below Laird certified table.
- 5) Why is Antenna Gain **setting** used? Implemented (in AT firmware) lower RF TX power (for both 20dBm and 10dBm modes) than certified in 10dBm mode. Reason for this is the 10dBm mode TX power setting is hardcoded to 10dBm (by Silabs), so to achieve Laird certified TX power e.g. 7dBm for CE (which is lower than 10dBm for CE), the method of using Antenna Gain **setting** is used to produce the actual TX power that Laird certified in the 10dBm mode. Since Antenna Gain **setting** applies to both 10dBm mode and 20dBm mode and all countries, so it impacts RF TX power across both modes (20dBm and 10dBm modes) and countries.
Silabs BLE SDK 5.0.0.0 GA (December 14, 2022) version does NOT allow TX power setting in 10dBm mode to be modified.

13.2.4 Europe (CE), UK (UKCA), Australia (RCM, New Zealand (RCM) Radio RF TX power Table

Table 30: 20dBm mode - Europe (CE), UK (UKCA), Australia (RCM, New Zealand (RCM) Radio TX power table

Module Laird Part number	453-00148							
Description	Lyra 24P - Bluetooth v5.4 PCB Module (20dBm) with RF Trace Pad (Silicon Labs EFR32BG24)							
Antenna Gain (dBi)	2.0dBi peak external antenna							
Radio Regulatory country:	Europe (CE), UK (UKCA), Australia (RCM) and New Zealand (RCM)							
Declared as FHSS or DTS?	FHSS (uses Silabs AFH FW module ON)							
AFH FW module?	AFH firmware module turned ON.							
Silabs BLE SDK:	5.0.0.0 GA (December 14, 2022).							
Silabs Gecko SDK Suite:	4.2 (December 14, 2022).							
20dBm mode. Declared as FHSS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	Conducted TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	17dBm	17.41dBm	17dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	17dBm	17.14 dBm	17dBm	17dBm	3.5dBi	20dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	17dBm	17.44dBm	17dBm	17dBm	3.5dBi	20dBm
	CH38 (CH36)	2478 MHz	17dBm	17.22dBm	17dBm	17dBm	3.5dBi	20dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	17dBm	17.40dBm	17dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	17dBm	17.10dBm	17dBm	17dBm	3.5dBi	20dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	17dBm	17.40dBm	17dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	17dBm	17.15dBm	17dBm	17dBm	3.5dBi	20dBm

Table 31: 10dBm mode - Europe (CE), UK (UKCA), Australia (RCM, New Zealand (RCM) Radio TX power table

10dBm mode. Declared as DTS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	7dBm	7.58dBm	7dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	7dBm	7.20dBm	7dBm	7dBm	3.5dBi	10dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	7dBm	7.59dBm	7dBm	7dBm	3.5dBi	10dBm
	CH38 (CH36)	2478 MHz	7dBm	7.25dBm	7dBm	7dBm	3.5dBi	10dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	7dBm	7.58dBm	7dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	7dBm	7.20dBm	7dBm	7dBm	3.5dBi	10dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	7dBm	7.58dBm	7dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	7dBm	7.20dBm	7dBm	7dBm	3.5dBi	10dBm

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY in 20dBm mode or 10dBm mode tables. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's. This lowest common TX power setting is stated since we do not use **per BLE** RF TX power setting in AT firmware, but same TX power setting across all 4 BLE PHY's.

NOTE3: IMPLEMENT in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. For CE, UKCA, RCM (Australia and New Zealand), this is actual target 17dBm conducted (in 20dBm mode) and 7dBm conducted (in 10dBm mode). To implement that, NOTE4A defines what Antenna Gain setting MUST be used and NOTE4B defines what TX power setting MUST be used.

NOTE4: IMPLEMENTED in AT firmware (or MUST implement in customers own developed C-code) the Actual target RF TX power conducted:

NOTE4A: the Antenna Gain **setting** of 3.5dBi and

NOTE4B: the TX power **setting** to 20dBm (in 20dBm mode) and 10dBm (in 10dBm mode).

which results in:

Target Actual RF TX power (dBm) = TX power **setting** (dBm) - Antenna Gain **setting**(dBi)

17dBm = 20dBm – 3.5dBi

7dBm = 10dBm – 3.5dBi

13.2.5 USA (FCC), Canada (ISED) Radio RF TX power Table

Table 32: 20dBm mode - USA (FCC), Canada (ISED) Radio TX power table

Module Laird Part number		453-00148						
Description		Lyra 24P - Bluetooth v5.4 PCB Module (20dBm) with RF Trace Pad (Silicon Labs EFR32BG24)						
Antenna Gain (dBi)		2.0dBi peak external antenna						
Radio Regulatory country:		USA (FCC), CANADA (ISED)						
Declared as FHSS or DTS?		FHSS (uses Silabs AFH FW module ON)						
AFH FW module?		AFH firmware module turned ON.						
Silabs BLE SDK:		5.0.0.0 GA (December 14, 2022).						
Silabs Gecko SDK Suite:		4.2 (December 14, 2022).						
20dBm mode. FHSS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1				NOTE2	NOTE3	NOTE4A	NOTE4B
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402MHz	20dBm	19.95dBm	17dBm	17dBm	3.5dBi	20dBm
	CH19 (CH17)	2440MHz	20dBm	19.93dBm	17dBm	17dBm	3.5dBi	20dBm
	CH38 (CH36)	2478MHz	18dBm	18.10dBm	17dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480MHz	15dBm	15.53dBm	Turn OFF CH39 (2480MHz)	Turn OFF CH39 (2480MHz) in FW.		
BLE 2Mbps	CH1 (CH0)	2404MHz	20dBm	19.94dBm	17dBm	17dBm	3.5dBi	20dBm
	CH19 (CH17)	2440MHz	20dBm	19.92dBm	17dBm	17dBm	3.5dBi	20dBm
	CH38 (CH36)	2478MHz	17dBm	17.21dBm	17dBm	17dBm	3.5dBi	20dBm
BLE coded PHY 125kbps	CH0 (CH37)	2402MHz	20dBm	19.94dBm	17dBm	17dBm	3.5dBi	20dBm
	CH19 (CH17)	2440MHz	20dBm	19.91dBm	17dBm	17dBm	3.5dBi	20dBm
	CH38 (CH36)	2478MHz	18dBm	18.09dBm	17dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480MHz	15dBm	15.52dBm	Turn OFF CH39 (2480MHz)	Turn OFF CH39 (2480MHz) in FW.		
BLE coded PHY 500kbps	CH0 (CH37)	2402MHz	20dBm	19.93dBm	17dBm	17dBm	3.5dBi	20dBm
	CH19 (CH17)	2440MHz	20dBm	19.90dBm	17dBm	17dBm	3.5dBi	20dBm
	CH38 (CH36)	2478MHz	18dBm	18.08dBm	17dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480MHz	15dBm	15.51dBm	Turn OFF CH39 (2480MHz)	Turn OFF CH39 (2480MHz) in FW.		

Table 33: 10dBm mode - USA (FCC), Canada (ISED) Radio TX power table

10dBm mode. DTS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	Implemented in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1				NOTE2	NOTE3	NOTE4A	NOTE4B
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402MHz	10dBm	10.32dBm	10dBm	7dBm	3.5dBi	10dBm
	CH19 (CH17)	2440MHz	10dBm	10.18dBm	10dBm	7dBm	3.5dBi	10dBm
	CH38 (CH36)	2478MHz	10dBm	10.05dBm	10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480MHz	10dBm	10.02dBm	10dBm	7dBm	3.5dBi	10dBm
BLE 2Mbps	CH1 (CH0)	2404MHz	10dBm	10.31dBm	10dBm	7dBm	3.5dBi	10dBm
	CH19 (CH17)	2440MHz	10dBm	10.17dBm	10dBm	7dBm	3.5dBi	10dBm

BLE coded PHY 125kbps	CH38 (CH36)	2478MHz	10dBm	10.03dBm	10dBm	7dBm	3.5dBi	10dBm
	CH0 (CH37)	2402MHz	10dBm	10.30dBm	10dBm	7dBm	3.5dBi	10dBm
	CH19 (CH17)	2440MHz	10dBm	10.17dBm	10dBm	7dBm	3.5dBi	10dBm
	CH38 (CH36)	2478MHz	10dBm	10.02dBm	10dBm	7dBm	3.5dBi	10dBm
BLE coded PHY 500kbps	CH39 (CH39)	2480MHz	10dBm	10.01dBm	10dBm	7dBm	3.5dBi	10dBm
	CH0 (CH37)	2402MHz	10dBm	10.29dBm	10dBm	7dBm	3.5dBi	10dBm
	CH19 (CH17)	2440MHz	10dBm	10.16dBm	10dBm	7dBm	3.5dBi	10dBm
	CH38 (CH36)	2478MHz	10dBm	10.02dBm	10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480MHz	10dBm	10.01dBm	10dBm	7dBm	3.5dBi	10dBm

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY in 20dBm mode or 10dBm mode tables. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's is **17dBm AND BLE CH39 2480MHz is turned OFF**. Why do we turn OFF BLE CH39 2480MHz is because the CH39 2480MHz RF TX power that FCC, ISED pass was achieved at 15dBm, which is lower than 17dBm achieved at some of the other BLE channels. To use the lowest common RF TX power setting of 17dBm AND MUST turn OFF BLE channel CH39 2480MHz.

NOTE3: IMPLEMENT in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. For FCC (USA), ISED (Canada), this is actual 17dBm conducted (in 20dBm mode) and 7dBm conducted (in 10dBm mode). To implement that, NOTE4A defines what Antenna Gain setting MUST be used and NOTE4B defines what TX power setting MUST be used.

NOTE4: IMPLEMENTED in AT firmware (or MUST implement in customers own developed C-code) the Actual target RF TX power conducted:

NOTE4A: the Antenna Gain **setting** of 3.5dBi and

NOTE4B: the TX power **setting** to 20dBm (in 20dBm mode) and 10dBm (in 10dBm mode).

which results in:

$$\text{Target Actual RF TX power (dBm)} = \text{TX power setting (dBm)} - \text{Antenna Gain setting (dBi)}$$

$$17\text{dBm} = 20\text{dBm} - 3.5\text{dBi}$$

$$7\text{dBm} = 10\text{dBm} - 3.5\text{dBi}$$

13.2.6 Australia (RCM, New Zealand (RCM) Radio RF TX power Table

Same as EU (CE). Refer to [Europe \(CE\)](#), [UK \(UKCA\)](#), [Australia \(RCM, New Zealand \(RCM\) Radio RF TX power Table](#).

13.2.7 Japan (MIC) Radio RF TX power Table

Table 34: 20dBm mode - Japan (MIC) Radio TX power table

Module Laird Part number	453-00148							
Description	Lyra 24P - Bluetooth v5.4 PCB Module (20dBm) with RF Trace Pad (Silicon Labs EFR32BG24)							
Antenna Gain (dBi)	2.0dBi peak external antenna							
Radio Regulatory country:	Japan (MIC)							
Declared as FHSS or DTS?	FHSS (uses Silabs AFH FW module ON)							
AFH FW module?	AFH firmware module turned ON.							
Silabs BLE SDK:	5.0.0.0 GA (December 14, 2022).							
Silabs Gecko SDK Suite:	4.2 (December 14, 2022).							
20dBm mode. FHSS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1							
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	Conducted TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	18dBm	18.50dBm	18dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	20dBm	17.54dBm	18dBm	17dBm	3.5dBi	20dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	18dBm	18.22dBm	18dBm	17dBm	3.5dBi	20dBm
	CH38 (CH36)	2478 MHz	18dBm	18.02dBm	18dBm	17dBm	3.5dBi	20dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	18dBm	18.49dBm	18dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	18dBm	18.30dBm	18dBm	17dBm	3.5dBi	20dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	18dBm	18.21dBm	18dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	18dBm	18.10dBm	18dBm	17dBm	3.5dBi	20dBm

Table 35: 10dBm mode - Japan (MIC) Radio TX power table

10dBm mode. DTS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1							
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	9dBm	9.76dBm	9dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	9dBm	9.48dBm	9dBm	7dBm	3.5dBi	10dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	9dBm	9.74dBm	9dBm	7dBm	3.5dBi	10dBm
	CH38 (CH36)	2478 MHz	9dBm	9.49dBm	9dBm	7dBm	3.5dBi	10dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	9dBm	9.73dBm	9dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	9dBm	9.43dBm	9dBm	7dBm	3.5dBi	10dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	9dBm	9.76dBm	9dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	9dBm	9.46dBm	9dBm	7dBm	3.5dBi	10dBm

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY in 20dBm mode or 10dBm mode tables. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's. This lowest common TX power setting is stated since we do not use **per BLE** RF TX power setting in AT firmware, but same TX power setting across all 4 BLE PHY's.

NOTE3: IMPLEMENT in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. For Japan, this is the actual target 17dBm conducted (in 20dBm mode) and 7dBm conducted (in 10dBm mode). To implement that, NOTE4A defines what Antenna Gain setting MUST be used and NOTE4B defines what TX power setting MUST be used.

NOTE4: IMPLEMENTED in AT firmware (or MUST implement in customers own developed C-code) the Actual target RF TX power conducted:

NOTE4A: the Antenna Gain **setting** of 3.5dBi and

NOTE4B: the TX power **setting** to 20dBm (in 20dBm mode) and 10dBm (in 10dBm mode).

which results in:

Target Actual RF TX power (dBm) = TX power **setting** (dBm) - Antenna Gain **setting**(dBi)

17dBm = 20dBm – 3.5dBi

7dBm = 10dBm – 3.5dBi

13.2.8 South Korea Radio RF TX power Table

Table 36: 20dBm mode - South Korea TX power table

Module Laird Part number	453-00148							
Description	Lyra 24P - Bluetooth v5.4 PCB Module (20dBm) with RF Trace Pad (Silicon Labs EFR32BG24)							
Antenna Gain (dBi)	2.0dBi peak external antenna							
Radio Regulatory country:	South Korea (SK)							
Declared as FHSS or DTS?	FHSS (uses Silabs AFH FW module ON)							
AFH FW module?	AFH firmware module turned ON.							
Silabs BLE SDK:	5.0.0.0 GA (December 14, 2022).							
Silabs Gecko SDK Suite:	4.2 (December 14, 2022).							
20dBm mode. FHSS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	Conducted TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	20dBm	19.89dBm	20dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	20dBm	17.23dBm	20dBm	17dBm	3.5dBi	20dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	20dBm	19.91dBm	20dBm	17dBm	3.5dBi	20dBm
	CH38 (CH36)	2478 MHz	20dBm	19.79dBm	20dBm	17dBm	3.5dBi	20dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	20dBm	19.88dBm	20dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	20dBm	19.25dBm	20dBm	17dBm	3.5dBi	20dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	20dBm	19.89dBm	20dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	20dBm	19.25dBm	20dBm	17dBm	3.5dBi	20dBm

Table 37: 10dBm mode – South Korea Radio TX power table

10dBm mode. DTS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
	CH38 (CH36)	2478 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY in 20dBm mode or 10dBm mode tables. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's. This lowest common TX power setting is stated since we do not use **per BLE** RF TX power setting in AT firmware, but same TX power setting across all 4 BLE PHY's.

NOTE3: IMPLEMENT in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. For South Korea, this is the actual target 17dBm conducted (in 20dBm mode) and 7dBm conducted (in 10dBm mode). To implement that, NOTE4A defines what Antenna Gain setting **MUST** be used and NOTE4B defines what TX power setting **MUST** be used.

NOTE4: IMPLEMENTED in AT firmware (or **MUST** implement in customers own developed C-code) the Actual target RF TX power conducted:

NOTE4A: the Antenna Gain **setting** of 3.5dBi and

NOTE4B: the TX power **setting** to 20dBm (in 20dBm mode) and 10dBm (in 10dBm mode).

which results in:

Target Actual RF TX power (dBm) = TX power **setting** (dBm) - Antenna Gain **setting**(dBi)

$$17\text{dBm} = 20\text{dBm} - 3.5\text{dBi}$$

$$7\text{dBm} = 10\text{dBm} - 3.5\text{dBi}$$

13.2.9 Global (lowest common across certified countries) Radio RF TX power Table

Same as EU (CE) [AND additionally BLE CH39 2480MHz turned OFF](#). Refer to [Europe \(CE\)](#), [UK \(UKCA\)](#), [Australia \(RCM\)](#), [New Zealand \(RCM\)](#) Radio RF TX power Table.

13.3 Maximum Regulatory Certified RF TX Power per Country – 453-00145 Lyra 24P – Bluetooth v5.4 PCB Module (20dBm) with Integrated Antenna

13.3.1 For shipped AT firmware

AT firmware implements RF TX power settings per country highlighted below sections.

	Country	Global	EU	UK	USA	Canada	Australia	New Zealand	Japan	South Korea
AT FW	Region code	GL	EU	UK	US	CA	AU	NZ	JP	SK
AFH?	Turned on or off?	on	on	on	on	on	on	on	on	on
20dBm mode	Target TX power conducted	17dBm	17dBm	17dBm	17dBm	17dBm	17dBm	17dBm	17dBm	17dBm
	Antenna Gain setting .	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi
	NOTES									
	TX power setting	20dBm	20dBm	20dBm	20dBm	20dBm	20dBm	20dBm	20dBm	20dBm
	Turn off CH39 2480MHz?	no	no	no	no	no	no	no	no	no
10dBm mode	Target TX power conducted	7dBm	7dBm	7dBm	7dBm	7dBm	7dBm	7dBm	7dBm	7dBm
	Antenna Gain setting	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi	3.5dBi
	TX power setting	10dBm	10dBm	10dBm	10dBm	10dBm	10dBm	10dBm	10dBm	10dBm

453-00145 Lyra 24P – Bluetooth v5.4 PCB Module (20dBm) with Integrated Antenna when loaded with AT firmware where the radio regulatory region “global” is set which is lowest common settings across RF TX power across certified countries. To switch to the specific radio regulatory region country of USA, Canada, Europe, UK, Australia, New Zealand, Japan and South Korea, customer can use appropriate AT command for setting the radio regulatory region per country.

13.3.2 For customers C code development

Customers developing with **C Code** – Full software development with Silicon Labs SDK and Toolchain, MUST implement the maximum RF TX power settings per country and other parameters mentioned in this section.

13.3.3 AFH firmware module description

See section [AFH firmware module](#).

13.3.4 Europe (CE), UK (UKCA), Australia (RCM, New Zealand (RCM) Radio RF TX power Table

Table 38: 20dBm mode - Europe (CE), UK (UKCA), Australia (RCM, New Zealand (RCM) Radio TX power table

Module Laird Part number	453-00145							
Description	Lyra 24P - Bluetooth v5.4 PCB Module (20dBm) with integrated antenna (Silicon Labs EFR32BG24)							
Antenna Gain (dBi)	1.82dBi peak							
Radio Regulatory country:	Europe (CE), UK (UKCA), Australia (RCM) and New Zealand (RCM)							
Declared as FHSS or DTS?	FHSS (uses Silabs AFH FW module ON)							
AFH FW module?	AFH firmware module turned ON.							
Silabs BLE SDK:	5.0.0.0 GA (December 14, 2022).							
Silabs Gecko SDK Suite:	4.2 (December 14, 2022).							
20dBm mode. FHSS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	Conducted TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	17dBm	17.41dBm	17dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	17dBm	17.14 dBm	17dBm	17dBm	3.5dBi	20dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	17dBm	17.44dBm	17dBm	17dBm	3.5dBi	20dBm
	CH38 (CH36)	2478 MHz	17dBm	17.22dBm	17dBm	17dBm	3.5dBi	20dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	17dBm	17.40dBm	17dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	17dBm	17.10dBm	17dBm	17dBm	3.5dBi	20dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	17dBm	17.40dBm	17dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	17dBm	17.15dBm	17dBm	17dBm	3.5dBi	20dBm

Table 39: 10dBm mode - Europe (CE), UK (UKCA), Australia (RCM, New Zealand (RCM) Radio TX power table

10dBm mode. DTS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	7dBm	7.43dBm	7dBm	7dBm	3.5dBi	10dBm
	CH19 (CH17)	2440 MHz	8dBm	8.13dBm	7dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	8dBm	7.99dBm	7dBm	7dBm	3.5dBi	10dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	7dBm	7.44dBm	7dBm	7dBm	3.5dBi	10dBm
	CH19 (CH17)	2440 MHz	7dBm	7.27dBm	7dBm	7dBm	3.5dBi	10dBm
	CH38 (CH36)	2478 MHz	8dBm	8.03dBm	7dBm	7dBm	3.5dBi	10dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	7dBm	7.43dBm	7dBm	7dBm	3.5dBi	10dBm
	CH19 (CH17)	2440 MHz	8dBm	8.13dBm	7dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	8dBm	7.98dBm	7dBm	7dBm	3.5dBi	10dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	7dBm	7.43dBm	7dBm	7dBm	3.5dBi	10dBm
	CH19 (CH17)	2440 MHz	8dBm	8.13dBm	7dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	8dBm	7.99dBm	7dBm	7dBm	3.5dBi	10dBm

Each column of the table has NOTE reference and these NOTES are:

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY in 20dBm mode or 10dBm mode tables. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's. This lowest common TX power setting is stated since we do not use **per BLE** RF TX power setting in AT firmware, but same TX power setting across all 4 BLE PHY's.

NOTE3: IMPLEMENTED in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. So for CE, UKCA, RCM (Australia and New Zealand), this is actual target 17dBm conducted (in 20dBm mode) and 7dBm conducted (in 10dBm mode). To implement that, NOTE4A defines what Antenna Gain setting MUST be used and NOTE4B defines what TX power setting MUST be used.

NOTE4: IMPLEMENTED in AT firmware (or MUST implement in customers own developed C-code) the Actual target RF TX power conducted:-

NOTE4A: the Antenna Gain **setting** of 3.5dBi and

NOTE4B: the TX power **setting** to 20dBm (in 20dBm mode) and 10dBm (in 10dBm mode).

which results in:

Target Actual RF TX power (dBm) = TX power **setting** (dBm) - Antenna Gain **setting**(dBi)

$$17\text{dBm} = 20\text{dBm} - 3.5\text{dBi}$$

$$7\text{dBm} = 10\text{dBm} - 3.5\text{dBi}$$

13.3.5 USA (FCC), Canada (ISED) Radio RF TX power Table

Table 40: 20dBm mode - Usa (FCC), Canada (ISED) Radio TX power table

Module Laird Part number	453-00145							
Description	Lyra 24P - Bluetooth v5.4 PCB Module (20dBm) with integrated antenna (Silicon Labs EFR32BG24)							
Antenna Gain (dBi)	1.82dBi peak							
Radio Regulatory country:	USA (FCC), CANADA (ISED)							
Declared as FHSS or DTS?	FHSS (uses Silabs AFH FW module ON)							
AFH FW module?	AFH firmware module turned ON.							
Silabs BLE SDK:	5.0.0.0 GA (December 14, 2022).							
Silabs Gecko SDK Suite:	4.2 (December 14, 2022).							
20dBm mode. FHSS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	20dBm	19.63dBm	20dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	20dBm	17.12dBm	20dBm	17dBm	3.5dBi	20dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	20dBm	19.62dBm	20dBm	17dBm	3.5dBi	20dBm
	CH38 (CH36)	2478 MHz	20dBm	19.45dBm	20dBm	17dBm	3.5dBi	20dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	20dBm	19.62dBm	20dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	20dBm	19.23dBm	20dBm	17dBm	3.5dBi	20dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	20dBm	19.61dBm	20dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	20dBm	19.22dBm	20dBm	17dBm	3.5dBi	20dBm

Table 41: 10dBm mode - Usa (FCC), Canada (ISED) Radio TX power table

10dBm mode. DTS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	Implemented in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	10dBm	9.83dBm	10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.31dBm	10dBm	7dBm	3.5dBi	10dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	10dBm	9.82dBm	10dBm	7dBm	3.5dBi	10dBm
	CH38 (CH36)	2478 MHz	10dBm	9.30dBm	10dBm	7dBm	3.5dBi	10dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	10dBm	9.81dBm	10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.47dBm	10dBm	7dBm	3.5dBi	10dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	10dBm	9.79dBm	10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.28dBm	10dBm	7dBm	3.5dBi	10dBm

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY in 20dBm mode or 10dBm mode tables. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's is **17dBm AND BLE CH39 2480MHz is turned OFF**. Why do we turn OFF BLE CH39 2480MHz is because the CH39 2480MHz RF TX power that FCC, ISED pass was achieved at 15dBm, which is lower than 17dBm achieved at some of the other BLE channels. So, to use the lowest common RF TX power setting of 17dBm AND MUST turn OFF BLE channel CH39 2480MHz.

NOTE3: IMPLEMENT in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. So for FCC (USA), ISED (Canada), this is actual 17dBm conducted (in 20dBm mode) and 7dBm conducted (in 10dBm mode). To implement that, NOTE4A defines what Antenna Gain setting MUST be used and NOTE4B defines what TX power setting MUST be used.

NOTE4: IMPLEMENTED in AT firmware (or MUST implement in customers own developed C-code) the Actual target RF TX power conducted:-

NOTE4A: the Antenna Gain **setting** of 3.5dBi and

NOTE4B: the TX power **setting** to 20dBm (in 20dBm mode) and 10dBm (in 10dBm mode).

which results in:

Target Actual RF TX power (dBm) = TX power **setting** (dBm) - Antenna Gain **setting**(dBi)

$$17\text{dBm} = 20\text{dBm} - 3.5\text{dBi}$$

$$7\text{dBm} = 10\text{dBm} - 3.5\text{dBi}$$

13.3.6 Japan (MIC) Radio RF TX power Table

Table 42: 20dBm mode - Japan (MIC) Radio TX power table

Module Laird Part number	453-00145							
Description	Lyra 24P - Bluetooth v5.4 PCB Module (20dBm) with integrated antenna (Silicon Labs EFR32BG24)							
Antenna Gain (dBi)	1.82dBi peak							
Radio Regulatory country:	Japan (MIC)							
Declared as FHSS or DTS?	FHSS (uses Silabs AFH FW module ON)							
AFH FW module?	AFH firmware module turned ON.							
Silabs BLE SDK:	5.0.0.0 GA (December 14, 2022).							
Silabs Gecko SDK Suite:	4.2 (December 14, 2022).							
20dBm mode. FHSS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	18dBm	18.19dBm	18dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	20dBm	17.66dBm	18dBm	17dBm	3.5dBi	20dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	18dBm	18.16dBm	18dBm	17dBm	3.5dBi	20dBm
	CH38 (CH36)	2478 MHz	18dBm	18.05dBm	18dBm	17dBm	3.5dBi	20dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	18dBm	18.12dBm	18dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	18dBm	17.96dBm	18dBm	17dBm	3.5dBi	20dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	18dBm	18.12dBm	18dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	18dBm	17.95dBm	18dBm	17dBm	3.5dBi	20dBm

Table 43: 10dBm mode - Japan (MIC) Radio TX power table

10dBm mode. DTS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	Implemented in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	10dBm	9.65dBm	10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.43dBm	10dBm	7dBm	3.5dBi	10dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	10dBm	9.63dBm	10dBm	7dBm	3.5dBi	10dBm
	CH38 (CH36)	2478 MHz	10dBm	9.44dBm	10dBm	7dBm	3.5dBi	10dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	10dBm	9.62dBm	10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.42dBm	10dBm	7dBm	3.5dBi	10dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	10dBm	9.64dBm	10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.45dBm	10dBm	7dBm	3.5dBi	10dBm

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY in 20dBm mode or 10dBm mode tables. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's. This lowest common TX power setting is stated since we do not use **per BLE** RF TX power setting in AT firmware, but same TX power setting across all 4 BLE PHY's.

NOTE3: IMPLEMENT in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. So for Japan, this is the actual target 17dBm conducted (in 20dBm mode) and 7dBm conducted (in 10dBm mode). To implement that, NOTE4A defines what Antenna Gain setting MUST be used and NOTE4B defines what TX power setting MUST be used.

NOTE4: IMPLEMENTED in AT firmware (or MUST implement in customers own developed C-code) the Actual target RF TX power conducted:-

NOTE4A: the Antenna Gain **setting** of 3.5dBi and

NOTE4B: the TX power **setting** to 20dBm (in 20dBm mode) and 10dBm (in 10dBm mode).

which results in:

Target Actual RF TX power (dBm) = TX power **setting** (dBm) - Antenna Gain **setting**(dBi)

$$17\text{dBm} = 20\text{dBm} - 3.5\text{dBi}$$

$$7\text{dBm} = 10\text{dBm} - 3.5\text{dBi}$$

13.3.7 South Korea Radio RF TX power Table

Table 44: 20dBm mode – South Korea Radio TX power table

Module Laird Part number	453-00145							
Description	Lyra 24P - Bluetooth v5.4 PCB Module (20dBm) with integrated antenna (Silicon Labs EFR32BG24)							
Antenna Gain (dBi)	1.82dBi peak							
Radio Regulatory country:	South Korea							
Declared as FHSS or DTS?	FHSS (uses Silabs AFH FW module ON)							
AFH FW module?	AFH firmware module turned ON.							
Silabs BLE SDK:	5.0.0.0 GA (December 14, 2022).							
Silabs Gecko SDK Suite:	4.2 (December 14, 2022).							
20dBm mode. FHSS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	20dBm	19.22dBm	20dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	20dBm	16.77dBm	20dBm	17dBm	3.5dBi	20dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	20dBm	19.28dBm	20dBm	17dBm	3.5dBi	20dBm
	CH38 (CH36)	2478 MHz	20dBm	19.26dBm	20dBm	17dBm	3.5dBi	20dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	20dBm	19.27dBm	20dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	20dBm	18.73dBm	20dBm	17dBm	3.5dBi	20dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	20dBm	19.26dBm	20dBm	17dBm	3.5dBi	20dBm
	CH39 (CH39)	2480 MHz	20dBm	18.76dBm	20dBm	17dBm	3.5dBi	20dBm

Table 45: 10dBm mode – South Korea Radio TX power table

10dBm mode. DTS.	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	Implemented in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code.		
	NOTE1					NOTE2	NOTE3	NOTE4A
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified Measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
	CH38 (CH36)	2478 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm		10dBm	7dBm	3.5dBi	10dBm

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY in 20dBm mode or 10dBm mode tables. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's. This lowest common TX power setting is stated since we do not use **per BLE** RF TX power setting in AT firmware, but same TX power setting across all 4 BLE PHY's.

NOTE3: IMPLEMENT in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. So for South Korea, this is the actual target 17dBm conducted (in 20dBm mode) and 7dBm conducted (in 10dBm mode). To implement that, NOTE4A defines what Antenna Gain setting MUST be used and NOTE4B defines what TX power setting MUST be used.

NOTE4: IMPLEMENTED in AT firmware (or MUST implement in customers own developed C-code) the Actual target RF TX power conducted:-

NOTE4A: the Antenna Gain **setting** of 3.5dBi and

NOTE4B: the TX power **setting** to 20dBm (in 20dBm mode) and 10dBm (in 10dBm mode).

which results in:

Target Actual RF TX power (dBm) = TX power **setting** (dBm) - Antenna Gain **setting**(dBi)

$$17\text{dBm} = 20\text{dBm} - 3.5\text{dBi}$$

$$7\text{dBm} = 10\text{dBm} - 3.5\text{dBi}$$

13.3.8 Global (lowest common across certified countries) Radio RF TX power Table

Same as EU (CE). Refer to [Europe \(CE\)](#), [UK \(UKCA\)](#), [Australia \(RCM\)](#), [New Zealand \(RCM\)](#) Radio RF TX power Table.

13.4 Maximum Regulatory Certified RF TX Power per Country – 453-00184 Lyra 24P – Bluetooth v5.4 USB Adaptor (20dBm) with Integrated Antenna

The Lyra 24P USB adaptor uses the 453-000145 - Lyra 24P Series - Bluetooth v5.4 PCB Module (20dBm) with integrated antenna module. The maximum regulatory certified TX power per country for the 453-00184 Lyra 24P – Bluetooth v5.4 USB Adaptor with Integrated Antenna is the same as the [Maximum Regulatory Certified RF TX Power per Country – 453-00145 Lyra 24P – Bluetooth v5.4 PCB Module \(20dBm\) with Integrated Antenna](#).

The certifications for the Lyra 24 USB Adaptor are performed with the DCDC converter turned on only.

13.5 Maximum Regulatory Certified RF TX Power per Country – 453-00142 Lyra 24P – Bluetooth v5.4 PCB Module (10dBm) with Integrated Antenna

13.5.1 For shipped AT firmware

Laird Connectivity AT firmware implements maximum RF TX power settings per country highlighted below.

	Country	Global	EU	UK	USA	Canada	Australia	New Zealand	Japan	South Korea
AT FW	Region code	GL	EU	UK	US	CA	AU	NZ	JP	SK
AFH?	Turned on or off	off	off	off	off	off	off	off	off	off
10dBm mode	Target TX power conducted	7dBm	7dBm	7dBm	10dBm	10dBm	7dBm	7dBm	9dBm	10dBm
	Antenna Gain setting	0dBi	0dBi	0dBi	0dBi	0dBi	0dBi	0dBi	0dBi	0dBi
	TX power setting	7dBm	7dBm	7dBm	10dBm	10dBm	7dBm	7dBm	9dBm	10dBm

453-00142 Lyra 24P – Bluetooth v5.4 PCB Module (10dBm) with Integrated Antenna is shipped AT firmware where the radio regulatory region “global” is set which is lowest common settings across RF TX power across certified countries. To switch to the specific radio regulatory region country of USA, Canada, Europe, UK, Australia, New Zealand, Japan and South Korea, customer can use appropriate AT command for setting the radio regulatory region per country.

13.5.2 For customers C code development

Customers developing with **C Code** – Full software development with Silicon Labs SDK and Toolchain, MUST implement the maximum RF TX power settings per country and other parameters mentioned in this section.

13.5.3 AFH firmware module description

See section [AFH firmware module](#).

13.5.4 Europe (CE), UK (UKCA), Australia (RCM, New Zealand (RCM) Radio RF TX power Table

Table 46: Europe (CE), UK (UKCA), Australia (RCM, New Zealand (RCM) Radio TX power table

Module Laird Part number	453-00142							
Description	Lyra 24P - Bluetooth v5.4 PCB Module (10dBm) with integrated antenna (Silicon Labs EFR32BG24)							
Antenna Gain (dBi)	1.82dBi peak							
Radio Regulatory country:	Europe (CE), UK (UKCA), Australia (RCM) and New Zealand (RCM)							
Declared as FHSS or DTS?	DTS (uses Silabs AFH FW module ON to cover Adaptivity test)							
AFH FW module?	AFH firmware module turned ON.							
Silabs BLE SDK:	5.0.0.0 GA (December 14, 2022).							
Silabs Gecko SDK Suite:	4.2 (December 14, 2022).							
10dBm	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1							
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	Conducted TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	7dBm	7.75dBm	7dBm	7dBm	0dBi	7dBm
	CH39 (CH39)	2480 MHz	7dBm	7.66dBm	7dBm	7dBm	0dBi	7dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	7dBm	7.76dBm	7dBm	7dBm	0dBi	7dBm
	CH38 (CH36)	2478 MHz	7dBm	7.68dBm	7dBm	7dBm	0dBi	7dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	7dBm	7.75dBm	7dBm	7dBm	0dBi	7dBm
	CH39 (CH39)	2480 MHz	7dBm	7.66dBm	7dBm	7dBm	0dBi	7dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	7dBm	7.75dBm	7dBm	7dBm	0dBi	7dBm
	CH39 (CH39)	2480 MHz	7dBm	7.67dBm	7dBm	7dBm	0dBi	7dBm

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's. This lowest common TX power setting is stated since we do not use **per BLE** RF TX power setting in AT firmware, but same TX power setting across all 4 BLE PHY's.

NOTE3: IMPLEMENT in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. So for CE, UKCA, RCM (Australia and New Zealand), this is actual target 7dBm conducted. To implement that, NOTE4A defines what Antenna Gain setting **MUST** be used and NOTE4B defines what TX power setting **MUST** be used.

NOTE4: IMPLEMENTED in AT firmware (or **MUST** implement in customers own developed C-code) the Actual target RF TX power conducted:-

NOTE4A: the Antenna Gain **setting** of 0dBi and

NOTE4B: the TX power **setting** to 7dBm .

which results in:

Target Actual RF TX power (dBm) = TX power **setting** (dBm) - Antenna Gain **setting**(dBi)

$$7\text{dBm} = 7\text{dBm} - 0\text{dBi}$$

13.5.5 USA (FCC), Canada (ISED) Radio RF TX power Table

Table 47: Usa (FCC), Canada (ISED) Radio TX power table

Module Laird Part number	453-00142							
Description	Lyra 24P - Bluetooth v5.4 PCB Module (10dBm) with integrated antenna (Silicon Labs EFR32BG24)							
Antenna Gain (dBi)	1.82dBi peak							
Radio Regulatory country:	USA (FCC), Canada (ISED)							
Declared as FHSS or DTS?	DTS (Silabs AFH FW module OFF)							
AFH FW module?	AFH firmware module turned OFF.							
Silabs BLE SDK:	5.0.0.0 GA (December 14, 2022).							
Silabs Gecko SDK Suite:	4.2 (December 14, 2022).							
10dBm	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1							
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	Conducted TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	10dBm	9.91dBm	10dBm	10dBm	0dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.74dBm	10dBm	10dBm	0dBi	10dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	10dBm	9.90dBm	10dBm	10dBm	0dBi	10dBm
	CH38 (CH36)	2478 MHz	10dBm	9.74dBm	10dBm	10dBm	0dBi	10dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	10dBm	9.89dBm	10dBm	10dBm	0dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.73dBm	10dBm	10dBm	0dBi	10dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	10dBm	9.89dBm	10dBm	10dBm	0dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.72dBm	10dBm	10dBm	0dBi	10dBm

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's. This lowest common TX power setting is stated since we do not use **per BLE** RF TX power setting in AT firmware, but same TX power setting across all 4 BLE PHY's.

NOTE3: IMPLEMENT in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. So for FCC, ISED, this is actual target 7dBm conducted. To implement that, NOTE4A defines what Antenna Gain setting MUST be used and NOTE4B defines what TX power setting MUST be used.

NOTE4: IMPLEMENTED in AT firmware (or MUST implement in customers own developed C-code) the Actual target RF TX power conducted:-

NOTE4A: the Antenna Gain **setting** of 0dBi and

NOTE4B: the TX power **setting** to 7dBm .

which results in:

$$\text{Target Actual RF TX power (dBm)} = \text{TX power setting (dBm)} - \text{Antenna Gain setting(dBi)}$$

$$7\text{dBm} = 7\text{dBm} - 0\text{dBi}$$

13.5.6 Japan (MIC) Radio RF TX power Table

Table 48: Japan (MIC) Radio TX power table

Module Laird Part number	453-00142							
Description	Lyra 24P - Bluetooth v5.4 PCB Module (10dBm) with integrated antenna (Silicon Labs EFR32BG24)							
Antenna Gain (dBi)	1.82dBi peak							
Radio Regulatory country:	Japan (MIC)							
Declared as FHSS or DTS?	DTS (Silicon Labs AFH FW module OFF)							
AFH FW module?	AFH firmware module turned OFF.							
Silabs BLE SDK:	5.0.0.0 GA (December 14, 2022).							
Silabs Gecko SDK Suite:	4.2 (December 14, 2022).							
10dBm	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1							
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	Conducted TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	9dBm	8.63dBm	9dBm	9dBm	0dBi	9dBm
	CH39 (CH39)	2480 MHz	9dBm	8.49dBm	9dBm	9dBm	0dBi	9dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	9dBm	8.55dBm	9dBm	9dBm	0dBi	9dBm
	CH38 (CH36)	2478 MHz	9dBm	8.41dBm	9dBm	9dBm	0dBi	9dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	9dBm	8.69dBm	9dBm	9dBm	0dBi	9dBm
	CH39 (CH39)	2480 MHz	9dBm	8.56dBm	9dBm	9dBm	0dBi	9dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	9dBm	8.61dBm	9dBm	9dBm	0dBi	9dBm
	CH39 (CH39)	2480 MHz	9dBm	8.50dBm	9dBm	9dBm	0dBi	9dBm

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's. This lowest common TX power setting is stated since we do not use **per BLE** RF TX power setting in AT firmware, but same TX power setting across all 4 BLE PHY's.

NOTE3: IMPLEMENT in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. So for Japan (MIC), this is actual target 7dBm conducted. To implement that, NOTE4A defines what Antenna Gain setting MUST be used and NOTE4B defines what TX power setting MUST be used.

NOTE4: IMPLEMENTED in AT firmware (or MUST implement in customers own developed C-code) the Actual target RF TX power conducted:-

NOTE4A: the Antenna Gain **setting** of 0dBi and

NOTE4B: the TX power **setting** to 7dBm .

which results in:

$$\text{Target Actual RF TX power (dBm)} = \text{TX power setting (dBm)} - \text{Antenna Gain setting(dBi)}$$

$$7\text{dBm} = 7\text{dBm} - 0\text{dBi}$$

13.5.7 South Korea Radio RF TX power Table

Table 49: South Korea TX power table

Module Laird Part number	453-00142							
Description	Lyra 24P - Bluetooth v5.4 PCB Module (10dBm) with integrated antenna (Silicon Labs EFR32BG24)							
Antenna Gain (dBi)	1.82dBi peak							
Radio Regulatory country:	South Korea							
Declared as FHSS or DTS?	FHSS (Silabs AFH FW module ON)							
AFH FW module?	AFH firmware module turned ON.							
Silabs BLE SDK:	5.0.0.0 GA (December 14, 2022).							
Silabs Gecko SDK Suite:	4.2 (December 14, 2022).							
10dBm	CERTIFIED maximum conducted RF TX power per BLE PHY				CERTIFIED LOWEST COMMON RF TX power setting across BLE PHY's, other restrict...	IMPLEMENTED in Laird Connectivity AT FW or customer MUST implement in customers own developed C-code. AFH firmware module turned ON.		
	NOTE1							
BLE PHY	Physical channel (channel Index)	Frequency (MHz) channel centre.	Certified conducted Maximum TX Power setting dBm	Certified measured Conducted Peak POWER (dBm)	Certified Lowest common conducted RF TX power setting across all 4 BLE data rates.	Target RF TX power conducted to implement in FW. Other restrictions (if any).	Antenna Gain setting in FW	Conducted TX power setting in FW
BLE 1Mbps	CH0 (CH37)	2402 MHz	10dBm	9.95dBm	10dBm	10dBm	0dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.88dBm	10dBm	10dBm	0dBi	10dBm
BLE 2Mbps	CH1 (CH0)	2404 MHz	10dBm	9.94dBm	10dBm	10dBm	0dBi	10dBm
	CH38 (CH36)	2478 MHz	10dBm	9.87dBm	10dBm	10dBm	0dBi	10dBm
BLE 125kbps	CH0 (CH37)	2402 MHz	10dBm	9.96dBm	10dBm	10dBm	0dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.88dBm	10dBm	10dBm	0dBi	10dBm
BLE 500kbps	CH0 (CH37)	2402 MHz	10dBm	9.95dBm	10dBm	10dBm	0dBi	10dBm
	CH39 (CH39)	2480 MHz	10dBm	9.87dBm	10dBm	10dBm	0dBi	10dBm

NOTE1: CERTIFIED maximum conducted RF TX power per BLE PHY. This is not what is implemented in AT firmware, this is what was certified only.

NOTE2: Certified Lowest common TX power setting across BLE PHY's. This lowest common TX power setting is stated since we do not use **per BLE** RF TX power setting in AT firmware, but same TX power setting across all 4 BLE PHY's.

NOTE3: IMPLEMENT in AT firmware **target** RF TX power conducted. This target actual implemented in AT firmware. So for South Korea, this is actual target 7dBm conducted. To implement that, NOTE4A defines what Antenna Gain setting **MUST** be used and NOTE4B defines what TX power setting **MUST** be used.

NOTE4: IMPLEMENTED in AT firmware (or **MUST** implement in customers own developed C-code) the Actual target RF TX power conducted:-

NOTE4A: the Antenna Gain **setting** of 0dBi and

NOTE4B: the TX power **setting** to 7dBm .

which results in:

$$\text{Target Actual RF TX power (dBm)} = \text{TX power setting (dBm)} - \text{Antenna Gain setting(dBi)}$$

$$7\text{dBm} = 7\text{dBm} - 0\text{dBi}$$

13.5.8 Global (lowest common across certified countries) Radio RF TX power Table

Same as EU (CE). Refer to [Europe \(CE\)](#), [UK \(UKCA\)](#), [Australia \(RCM\)](#), [New Zealand \(RCM\)](#) Radio RF TX power Table

14 BLUETOOTH SIG QUALIFICATION

14.1 Overview

The Lyra 24 Series module is listed on the Bluetooth SIG website as a qualified End Product, using the combination of a RF-PHY and Host Stack Components.

Design Name	Owner	Declaration ID	QDID	Link to listing on the SIG website
Lyra 24	Laird Connectivity	D063149	221359	https://launchstudio.bluetooth.com/ListingDetails/192322

14.1.1 Referenced Qualified Components

Design Name	Owner	Reference QDID	Link to listing on the SIG website
EFR32BG24 and EFR32MG24RF-PHY	Silicon Laboratories	184327	https://launchstudio.bluetooth.com/ListingDetails/149435
Wireless Gecko LL and Host	Silicon Laboratories	216508	https://launchstudio.bluetooth.com/ListingDetails/187016

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to registered as a member of the Bluetooth SIG – <https://www.bluetooth.com/>

The following link provides a link to the Bluetooth Registration page: <https://www.bluetooth.org/login/register/>

For each Bluetooth Design, it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

<https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/qualification-listing-fees/>

To purchase a new Declaration ID for your design, please follow the link below, (login is required to access this page):

[Launch Studio - Manage Declaration ID \(bluetooth.com\)](#)

14.2 Qualification Steps When Referencing on End Product Listing

For this qualification, follow these steps:

6. To start a listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm
7. [Select Start the Bluetooth Qualification Process with No Required Testing.](#)
8. **Project Basics:**
 - Enter the Project Name (this can be the product name or the Bluetooth Design name).
 - For Referenced Qualified Designs, enter QDID 221359.
9. **Product Declaration:**
 - Enter the Listing Date (this can any date ranging from the date of entry up to 90 days after submission) – Your design is qualified immediately but the listing does not go public until the specified date.
10. Add End Product(s) – Each end product that references the qualified design (without modification) can be added in this section. The Bluetooth SIG requires that you add each individual model number separately.

11. Declaration ID:

- Select a Declaration ID from the list.

Important! To complete this step, you must have already paid your Bluetooth SIG Declaration ID fee. If you have not, refer to the Bluetooth SIG Qualification Overview section for instructions. You also have the option of clicking **Pay Declaration Fee** accessible from this step of the Bluetooth SIG Qualification process.

12. Review and Submit – With this, some automatic checks occur to ensure all sections are complete.

- Review all entered information and make corrections, if needed.
- Once you have reviewed your information, tick all of the check boxes and add your name to the signature page.
- Click **Signature Confirmed – Complete Project & Submit Product(s) for Qualification**.
(You will be asked to confirm to proceed with the final listing one more time)

13. Once the listing is confirmed please download the SDoC and place a copy in the compliance folder.

For further information, please refer to the following webpage:

<https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/>

15 ADDITIONAL INFORMATION

Please contact your local sales representative or our support team for further assistance:

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Website	www.lairdconnect.com/
Technical Support	www.lairdconnect.com/resources/support
Sales Contact	www.lairdconnect.com/contact

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Laird Connectivity's products are subject to standard [Terms & Conditions](#).

www.lairdconnect.com

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